Francisco Gamiz

List of Publications by Year
in descending order

372	4,707	117625	168389
papers	citations	34 h-index	53 g-index

384	384	384	2486
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Analysis of the Reformulated Source to Drain Tunneling Probability for Improving the Accuracy of a Multisubband Ensemble Monte Carlo Simulator. Micromachines, 2022, 13, 533.	2.9	0
2	Improved inter-device variability in graphene liquid gate sensors by laser treatment. Solid-State Electronics, 2022, 192, 108259.	1.4	2
3	Influence of Punch Trough Stop Layer and Well Depths on the Robustness of Bulk FinFETs to Heavy Ions Impact. IEEE Access, 2022, 10, 47169-47178.	4.2	0
4	Performance of FDSOI double-gate dual-doped reconfigurable FETs. Solid-State Electronics, 2022, 194, 108336.	1.4	4
5	Memory Operation of ZÂ²-FET Without Selector at High Temperature. IEEE Journal of the Electron Devices Society, 2021, 9, 658-662.	2.1	2
6	Improved Retention Characteristics of Z2-FET Employing Half Back-Gate Control. IEEE Transactions on Electron Devices, 2021, 68, 1041-1044.	3.0	2
7	Hysteresis in As-Synthesized MoS2 Transistors: Origin and Sensing Perspectives. Micromachines, 2021, 12, 646.	2.9	3
8	Self-Consistent Enhanced S/D Tunneling Implementation in a 2D MS-EMC Nanodevice Simulator. Micromachines, 2021, 12, 601.	2.9	1
9	Metamaterial-Based Reconfigurable Intelligent Surface: 3D Meta-Atoms Controlled by Graphene Structures. IEEE Communications Magazine, 2021, 59, 42-48.	6.1	29
10	Performance and reliability in back-gated CVD-grown MoS2 devices. Solid-State Electronics, 2021, 186, 108173.	1.4	2
11	Synthesis of graphene and other two-dimensional materials. , 2021, , 1-79.		4
12	A Review of Sharp-Switching Band-Modulation Devices. Micromachines, 2021, 12, 1540.	2.9	3
13	Dual PN Source/Drain Reconfigurable FET for Fast and Low-Voltage Reprogrammable Logic. IEEE Access, 2020, 8, 132376-132381.	4.2	7
14	Active Radiation-Hardening Strategy in Bulk FinFETs. IEEE Access, 2020, 8, 201441-201449.	4.2	5
15	Investigating the transient response of Schottky barrier back-gated MoS₂ transistors. 2D Materials, 2020, 7, 025040.	4.4	13
16	Memory Operations of Zero Impact Ionization, Zero Subthreshold Swing FET Matrix Without Selectors. IEEE Electron Device Letters, 2020, 41, 361-364.	3.9	4
17	CVD-grown back-gated MoS2 transistors. , 2020, , .		1
18	Quantum Enhancement of a S/D Tunneling Model in a 2D MS-EMC Nanodevice Simulator: NEGF Comparison and Impact of Effective Mass Variation. Micromachines, 2020, 11, 204.	2.9	7

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19	Systematic Characterization of Random Telegraph Noise and Its Dependence with Magnetic Fields in MOSFET Devices. , 2020, , 135-174.		2
20	Efficient Implementation of S/D tunneling in 2D MS-EMC of Nanoelectronic Devices Including the Thickness Dependent Effective Mass. , 2020, , .		0
21	Multi-Subband Ensemble Monte Carlo Simulator for Nanodevices in the End of the Roadmap. Lecture Notes in Computer Science, 2020, , 438-445.	1.3	2
22	Techniques for Statistical Enhancement in a 2D Multi-subband Ensemble Monte Carlo Nanodevice Simulator. Lecture Notes in Computer Science, 2020, , 411-419.	1.3	0
23	Capacitor-less dynamic random access memory based on a IIIâ€“V transistor with a gate length of 14â€‰nm. Nature Electronics, 2019, 2, 412-419.	26.0	27
24	3-D TCAD Study of the Implications of Channel Width and Interface States on FD-SOI Z²-FETs. IEEE Transactions on Electron Devices, 2019, 66, 2513-2519.	3.0	8
25	This special issue is devoted to selected papers presented at the EuroSOI-ULIS2018 international conference, held in Granada, Spain on 19â€“21 March 2018. Solid-State Electronics, 2019, 159, 1-2.	1.4	0
26	Capacitorless memory devices using virtual junctions. , 2019, , .		0
27	Near-field scanning microwave microscope platform based on a coaxial cavity resonator for the characterization of semiconductor structures. Solid-State Electronics, 2019, 159, 150-156.	1.4	8
28	Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell. IEEE Electron Device Letters, 2019, 40, 1084-1087.	3.9	10
29	Characteristics of band modulation FET on sub 10 nm SOI. Japanese Journal of Applied Physics, 2019, 58, SBBB07.	1.5	2
30	Simulation Perspectives of Sub-1V Single-Supply Z²-FET 1T-DRAM Cells for Low-Power. IEEE Access, 2019, 7, 40279-40284.	4.2	8
31	Investigation of thin gate-stack Z2-FET devices as capacitor-less memory cells. Solid-State Electronics, 2019, 159, 12-18.	1.4	3
32	A thorough study of Si nanowire FETs with 3D Multi-Subband Ensemble Monte Carlo simulations. Solid-State Electronics, 2019, 159, 19-25.	1.4	2
33	On the Low-Frequency Noise Characterization of Z²-FET Devices. IEEE Access, 2019, 7, 42551-42556.	4.2	4
34	Temperature and Gate Leakage Influence on the Z2-FET Memory Operation. , 2019, , .		1
35	TCAD Analysis of III-V capacitor-less A2RAM cells. , 2019, , .		0
36	New material design of fast switching phase change memory as the benchmark for FD-SOI devices. , 2019, , .		0

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37	Impact of Effective Mass on Transport Properties and Direct Source-to-Drain Tunneling in Ultrascaled Double Gate Devices: a 2D Multi-Subband Ensemble Monte Carlo study. , 2019, , .		0
38	Thorough Understanding of Retention Time of Z2FET Memory Operation. IEEE Transactions on Electron Devices, 2019, 66, 383-388.	3.0	11
39	Multisubband Ensemble Monte Carlo Analysis of Tunneling Leakage Mechanisms in Ultrascaled FDSOI, DGSOI, and FinFET Devices. IEEE Transactions on Electron Devices, 2019, 66, 1145-1152.	3.0	12
40	Impact of the Trap Attributes on the Gate Leakage Mechanisms in a 2D MS-EMC Nanodevice Simulator. Lecture Notes in Computer Science, 2019, , 273-280.	1.3	3
41	Analysis of the Heterogate Electronâ€“Hole Bilayer Tunneling Field-Effect Transistor With Partially Doped Channels: Effects on Tunneling Distance Modulation and Occupancy Probabilities. IEEE Transactions on Electron Devices, 2018, 65, 339-346.	3.0	4
42	Multi-Subband Ensemble Monte Carlo simulations of scaled GAA MOSFETs. Solid-State Electronics, 2018, 143, 49-55.	1.4	4
43	Confinement-induced InAs/GaSb heterojunction electronâ€“hole bilayer tunneling field-effect transistor. Applied Physics Letters, 2018, 112, .	3.3	20
44	Experimental Demonstration of Operational Z²-FET Memory Matrix. IEEE Electron Device Letters, 2018, 39, 660-663.	3.9	21
45	A review of the Z 2 -FET 1T-DRAM memory: Operation mechanisms and key parameters. Solid-State Electronics, 2018, 143, 10-19.	1.4	36
46	3D multi-subband ensemble Monte Carlo simulation of ã€˜100ã€‰ and ã€˜110ã€‰ Si nanowire FETs. , 2018, , .		0
47	MSDRAM, A2RAM and Z²-FET performance benchmark for 1T-DRAM applications. , 2018, , .		8
48	MS-EMC vs. NEGF: A comparative study accounting for transport quantum corrections. , 2018, , .		9
49	Impact of Strain on S/D tunneling in FinFETs: a MS-EMC study. , 2018, , .		0
50	Source-to-Drain Tunneling Analysis in FDSOI, DGSOI, and FinFET Devices by Means of Multisubband Ensemble Monte Carlo. IEEE Transactions on Electron Devices, 2018, 65, 4740-4746.	3.0	11
51	Simulation study on Z2FET scalability, process optimization and their impact on performance. , 2018, , .		2
52	Z²-FET memory matrix in 28 nm FDSOI technology. , 2018, , .		2
53	Gate Leakage Tunneling Impact on the InAs/GaSb Heterojunction Electronâ€“Hole Bilayer Tunneling Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4679-4686.	3.0	8
54	Scaling FDSOI technology down to 7 nm â€” A physical modeling study based on 3D phase-space subband boltzmann transport. , 2018, , .		1

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55	Impact of electron effective mass variation on the performance of InAs/GaSb Electron-Hole Bilayer Tunneling Field-Effect Transistor. , 2018, , .		4
56	Evaluation of thin-oxide Z2-FET DRAM cell. , 2018, , .		7
57	Experimental Characterization of the Random Telegraph Noise Signature in MOSFETs Under the Influence of Magnetic Fields. IEEE Electron Device Letters, 2018, 39, 1054-1057.	3.9	2
58	Towards InGaAs MSDRAM Capacitor-Less Cells. ECS Transactions, 2018, 85, 195-200.	0.5	3
59	Near field scanning microwave microscope based on a coaxial cavity resonator for the characterization of semiconductor structures. , 2018, , .		0
60	InGaAs Capacitor-Less DRAM Cells TCAD Demonstration. IEEE Journal of the Electron Devices Society, 2018, 6, 884-892.	2.1	9
61	Mechanical and thermal properties of graphene modified asphalt binders. Construction and Building Materials, 2018, 180, 265-274.	7.2	101
62	Confinement orientation effects in S/D tunneling. Solid-State Electronics, 2017, 128, 48-53.	1.4	5
63	Implementation of Band-to-Band Tunneling Phenomena in a Multisubband Ensemble Monte Carlo Simulator: Application to Silicon TFETs. IEEE Transactions on Electron Devices, 2017, 64, 3084-3091.	3.0	9
64	Ultra-low power 1T-DRAM in FDSOI technology. Microelectronic Engineering, 2017, 178, 245-249.	2.4	11
65	Low-Power Z2-FET Capacitorless 1T-DRAM. , 2017, , .		15
66	Extended Analysis of the Z^{2} -FET: Operation as Capacitorless eDRAM. IEEE Transactions on Electron Devices, 2017, 64, 4486-4491.	3.0	34
67	Electrostatic performance of InSb, GaSb, Si and Ge p-channel nanowires. Journal Physics D: Applied Physics, 2017, 50, 495106.	2.8	3
68	Characterization of semiconductor structures using scanning microwave microscopy technique. , 2017, , .		1
69	Multi-Subband Ensemble Monte Carlo simulations of scaled GAA MOSFETs. , 2017, , .		0
70	Assessment of gate leakage mechanism utilizing Multi-Subband Ensemble Monte Carlo. , 2017, , .		4
71	The mystery of the Z2-FET 1T-DRAM memory. , 2017, , .		2
72	Insights on the Body Charging and Noise Generation by Impact Ionization in Fully Depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 5093-5098.	3.0	0

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73	Systematic method for electrical characterization of random telegraph noise in MOSFETs. Solid-State Electronics, 2017, 128, 115-120.	1.4	5
74	Three-dimensional multi-subband simulation of scaled FinFETs. , 2017, , .		1
75	Simulation based DC and dynamic behaviour characterization of Z2FET. , 2017, , .		6
76	${Z}^{extsf {2}}$ -FET as Capacitor-Less eDRAM Cell For High-Density Integration. IEEE Transactions on Electron Devices, 2017, 64, 4904-4909.	3.0	28
77	Multi-subband ensemble Monte Carlo study of tunneling leakage mechanisms. , 2017, , .		3
78	2D-TCAD simulation on retention time of Z2FET for DRAM application. , 2017, , .		7
79	Gate-induced vs. implanted body doping impact on Z²-FET DC operation. , 2017, , .		0
80	Band-to-band tunneling distance analysis in the heterogate electronâ€“hole bilayer tunnel field-effect transistor. Journal of Applied Physics, 2016, 119, .	2.5	2
81	Comment on â€œOptimization of a Pocketed Dual-Metal-Gate TFET by Means of TCAD Simulations Accounting for Quantization-Induced Bandgap Wideningâ€• IEEE Transactions on Electron Devices, 2016, 63, 5077-5078.	3.0	2
82	Competitive 1T-DRAM in 28 nm FDSOI technology for low-power embedded memory. , 2016, , .		8
83	Capacitor-less memory: Advances and challenges. , 2016, , .		4
84	Confinement orientation effects in S/D tunneling. , 2016, , .		2
85	Assessment of confinement-induced band-to-band tunneling leakage in the FinEHBTFET. , 2016, , .		6
86	Electrical characterization of Random Telegraph Noise in back-biased Ultrathin Silicon-On-Insulator MOSFETs. , 2016, , .		1
87	On the influence of the back-gate bias on InGaAs Trigate MOSFETs. , 2016, , .		0
88	Switching Behavior Constraint in the Heterogate Electronâ€“Hole Bilayer Tunnel FET: The Combined Interplay Between Quantum Confinement Effects and Asymmetric Configurations. IEEE Transactions on Electron Devices, 2016, 63, 2570-2576.	3.0	7
89	Electrical characterization and conductivity optimization of laser reduced graphene oxide on insulator using point-contact methods. RSC Advances, 2016, 6, 46231-46237.	3.6	16
90	Quantum Mechanical Confinement in the Fin Electron-Hole Bilayer Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2016, , 1-7.	3.0	3

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91	Multi-subband ensemble Monte Carlo study of band-to-band tunneling in silicon-based TFETs. , 2016, , .		2
92	Active charge collection strategy for radiation environment at device level. , 2016, , .		2
93	Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation. Solid-State Electronics, 2016, 117, 60-65.	1.4	17
94	Impact of non uniform strain configuration on transport properties for FD14+ devices. Solid-State Electronics, 2016, 115, 232-236.	1.4	2
95	Multi-Subband Ensemble Monte Carlo simulation of Si nanowire MOSFETs. , 2015, , .		8
96	Direct Characterization of Impact Ionization Current in Silicon-on-Insulator Body-Contacted MOSFETs. ECS Transactions, 2015, 66, 93-99.	0.5	2
97	(Invited) Special Memory Mechanisms in SOI Devices. ECS Transactions, 2015, 66, 201-210.	0.5	0
98	Impact of non uniform strain configuration on transport properties for FD14+ devices. , 2015, , .		0
99	Threshold voltage and on-current Variability related to interface traps spatial distribution. , 2015, , .		3
100	Determination of ad hoc deposited charge on bare SOI wafers. , 2015, , .		5
101	Comment on â€˜Germanium electronâ€“hole bilayer tunnel field-effect transistors with a symmetrically arranged double gateâ€™. Semiconductor Science and Technology, 2015, 30, 128001.	2.0	4
102	Sub-22nm scaling of UTB2SOI devices for Multi-V<inf>t</inf> applications. , 2015, , .		0
103	Effects of dietary choline availability on latent inhibition of flavor aversion learning. Nutritional Neuroscience, 2015, 18, 275-280.	3.1	2
104	Mobility and Capacitance Comparison in Scaled InGaAs Versus Si Trigate MOSFETs. IEEE Electron Device Letters, 2015, 36, 114-116.	3.9	12
105	Strain effects on effective masses for MoS₂monolayers. Journal of Physics: Conference Series, 2015, 609, 012008.	0.4	2
106	Simulation study of the electron mobility in few-layer MoS2 metalâ€“insulator-semiconductor field-effect transistors. Solid-State Electronics, 2015, 114, 30-34.	1.4	13
107	Assessment of pseudo-bilayer structures in the heterogate germanium electron-hole bilayer tunnel field-effect transistor. Applied Physics Letters, 2015, 106, .	3.3	14
108	Impact of the Back-Gate Biasing on Trigate MOSFET Electron Mobility. IEEE Transactions on Electron Devices, 2015, 62, 224-227.	3.0	12

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109	Role of the gate in ballistic nanowire SOI MOSFETs. Solid-State Electronics, 2015, 112, 24-28.	1.4	2
110	Tunability of effective masses on MoS2 monolayers. Microelectronic Engineering, 2015, 147, 302-305.	2.4	6
111	Impact of Asymmetric Configurations on the Heterogate Germanium Electron–Hole Bilayer Tunnel FET Including Quantum Confinement. IEEE Transactions on Electron Devices, 2015, 62, 3560-3566.	3.0	27
112	Analytic Potential and Charge Model of Semiconductor Quantum Wells. IEEE Transactions on Electron Devices, 2015, 62, 4186-4191.	3.0	10
113	The unexpected beneficial effect of the L-valley population on the electron mobility of GaAs nanowires. Applied Physics Letters, 2015, 106, .	3.3	3
114	Response to â€œComment on â€˜Assessment of field-induced quantum confinement in heterogate germanium electronâ€“hole bilayer tunnel field-effect transistorâ€™â€•[Appl. Phys. Lett. 106, 026102 (2015)]. Applied Physics Letters, 2015, 106, 026103.	3.3	2
115	Impact of S/D tunneling in ultrascaled devices, a Multi-Subband Ensemble Monte Carlo study. , 2015, , .		6
116	Analytic drain current model for IIIâ€“V cylindrical nanowire transistors. Journal of Applied Physics, 2015, 118, 044502.	2.5	14
117	Implicit versus explicit momentum relaxation time solution for semiconductor nanowires. Journal of Applied Physics, 2015, 118, 024504.	2.5	1
118	A new explicit and analytical model for square Gate-All-Around MOSFETs with rounded corners. Solid-State Electronics, 2015, 111, 180-187.	1.4	6
119	Experimental developments of A2RAM memory cells on SOI and bulk substrates. Solid-State Electronics, 2015, 103, 7-14.	1.4	18
120	A2RAM: Low-power 1T-DRAM memory cells compatible with planar and 3D SOI substrates. , 2014, , .		0
121	TCAD simulation of interface traps related variability in bulk decananometer mosfets. , 2014, , .		4
122	Influence of alloy disorder scattering on the hole mobility of SiGe nanowires. Journal of Applied Physics, 2014, 116, .	2.5	3
123	Assessment of field-induced quantum confinement in heterogate germanium electronâ€“hole bilayer tunnel field-effect transistor. Applied Physics Letters, 2014, 105, 082108.	3.3	38
124	Size-dependent electron mobility in InAs nanowires. , 2014, , .		0
125	A parallel deterministic solver for the SchrÃ¶dingerâ€“Poissonâ€“Boltzmann system in ultra-short DG-MOSFETs: Comparison with Monte-Carlo. Computers and Mathematics With Applications, 2014, 67, 1703-1721.	2.7	11
126	Analytical model for the threshold voltage of IIIâ€“V nanowire transistors including quantum effects. Solid-State Electronics, 2014, 92, 28-34.	1.4	3

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127	3D multi-subband ensemble Monte Carlo simulator of FinFETs and nanowire transistors. , 2014, , .		11
128	Theoretical interpretation of the electron mobility behavior in InAs nanowires. Journal of Applied Physics, 2014, 116, 174505.	2.5	9
129	Modeling the Channel Charge and Potential in Quasi-Ballistic Nanoscale Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 2640-2646.	3.0	12
130	In Situ Characterization of Bias Instability in Bare SOI Wafers by Pseudo-MOSFET Technique. IEEE Transactions on Device and Materials Reliability, 2014, 14, 878-883.	2.0	2
131	Tri-Dimensional A2-RAM Cell: Entering the Third Dimension. Engineering Materials, 2014, , 105-124.	0.6	0
132	Taste and olfactory status in a gourmand with a right amygdala lesion. Neurocase, 2014, 20, 421-433.	0.6	5
133	Analytical temperature dependent model for nanoscale double-gate MOSFETs reproducing advanced transport models. Solid-State Electronics, 2014, 98, 2-6.	1.4	4
134	MONTE-CARLO SIMULATION OF ULTRA-THIN FILM SILICON-ON-INSULATOR MOSFETs. Selected Topics in Electornics and Systems, 2014, , 1-32.	0.2	0
135	An analytical mobility model for square Gate-All-Around MOSFETs. Solid-State Electronics, 2013, 90, 18-22.	1.4	5
136	Analytical Gate Capacitance Modeling of IIIâ€“V Nanowire Transistors. IEEE Transactions on Electron Devices, 2013, 60, 1590-1599.	3.0	18
137	Two-band kâ€‰Â·â€‰p model for Si-(110) electron devices. Journal of Applied Physics, 2013, 114, 073706.	2.5	2
138	Bias-Engineered Mobility in Advanced FD-SOI MOSFETs. IEEE Electron Device Letters, 2013, 34, 840-842.	3.9	14
139	Ab initio validation of continuum models for Si/SiO<inf>2</inf> interfaces. , 2013, , .		0
140	Influence of the back-gate bias on the electron mobility of trigate MOSFETs. , 2013, , .		1
141	Analytical drain current model using temperature dependence model in nanoscale Double-Gate (DG) MOSFETs. , 2013, , .		1
142	An in-depth Monte Carlo study of low-field mobility in ultra-thin body DGMOSFETs for modeling purposes. Solid-State Electronics, 2013, 79, 92-97.	1.4	2
143	On the extension of ET-FDSOI roadmap for 22nm node and beyond. Solid-State Electronics, 2013, 90, 23-27.	1.4	23
144	A new characterization technique for SOI wafers: Split C(V) in pseudo-MOSFET configuration. Solid-State Electronics, 2013, 90, 127-133.	1.4	15

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145	Direct point-contact characterization of Bias instability on bare SOI wafers. , 2013, , .		1
146	Ab initio validation of continuum models parametrizations for ultrascaled SOI interfaces. Microelectronic Engineering, 2013, 109, 286-289.	2.4	3
147	Influence of the interface trap location on the performance and variability of ultra-scaled MOSFETs. Microelectronics Reliability, 2013, 53, 1243-1246.	1.7	13
148	Effective Capacitance Area for Pseudo-MOSFET Characterization of Bare SOI Wafers by Split-C(V) Measurements. ECS Journal of Solid State Science and Technology, 2013, 2, P529-P533.	1.8	0
149	Determination of Effective Capacitance Area for Pseudo-MOSFET Based Characterization of Bare SOI Wafers by Split-C(V) Measurements. ECS Transactions, 2013, 53, 209-217.	0.5	4
150	Optimisation and parallelisation of a 2D MOSFET multi-subband ensemble Monte Carlo simulator. International Journal of High Performance Computing Applications, 2013, 27, 483-492.	3.7	6
151	Non-parabolicity in Si-(110) nMOSFETs: Analytic and numerical results for the two-band k · p model. , 2013, , .		0
152	The effect of quantum confinement on tunneling field-effect transistors with high-Î° gate dielectric. Applied Physics Letters, 2013, 103, .	3.3	14
153	Effect of confined acoustic phonons on the electron mobility of rectangular nanowires. Applied Physics Letters, 2013, 103, .	3.3	8
154	Notice of Removal: Fabrication and validation of A2RAM memory cells on SOI and bulk substrates - Withdrawn. , 2013, , .		1
155	Improving subthreshold MSB-EMC simulations by dynamic particle weighting. , 2013, , .		1
156	Impact of back-gate biasing on effective field and mobility in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect-transistors. Journal of Applied Physics, 2013, 113, .	2.5	11
157	MONTE-CARLO SIMULATION OF ULTRA-THIN FILM SILICON-ON-INSULATOR MOSFETs. International Journal of High Speed Electronics and Systems, 2013, 22, 1350001.	0.7	0
158	An in-depth simulation study of thermal reset transitions in resistive switching memories. Journal of Applied Physics, 2013, 114, .	2.5	58
159	Spontaneous object recognition memory in aged rats: Complexity versus similarity. Learning and Memory, 2012, 19, 444-448.	1.3	18
160	ADVANCED CONCEPTS FOR FLOATING-BODY MEMORIES. International Journal of High Speed Electronics and Systems, 2012, 21, 1250002.	0.7	0
161	Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator. IEEE Electron Device Letters, 2012, 33, 1717-1719.	3.9	48
162	Multibranch mobility characterization: Evidence of carrier mobility enhancement by back-gate biasing in FD-SOI MOSFET. , 2012, , .		1

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163	Impact of effective capacitance area on the characterization of SOI Wafers by Split-C(V) in Pseudo-MOSFET configuration. , 2012, , .		2
164	3D Trigate 1T-DRAM Memory Cell for 2x nm Nodes. , 2012, , .		0
165	A 20nm low-power triple-gate multibody 1T-DRAM cell. , 2012, , .		2
166	Innovative capacitorless SOI DRAMs. , 2012, , .		1
167	Combined effect of mechanical stressors and channel orientation on mobility in FDSOI n and p MOSFETs. , 2012, , .		0
168	Experimental demonstration of A2RAM memory cell on SOI. , 2012, , .		1
169	Effect of interfacial states on the technological variability of trigate MOSFETs. , 2012, , .		0
170	Accurate Calculation of Gate Tunneling Current in Double-Gate and Single-Gate SOI MOSFETs Through Gate Dielectric Stacks. IEEE Transactions on Electron Devices, 2012, 59, 2589-2596.	3.0	9
171	Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs. IEEE Transactions on Electron Devices, 2012, 59, 3205-3211.	3.0	38
172	A Simple Approach to Quantum Confinement in Tunneling Field-Effect Transistors. IEEE Electron Device Letters, 2012, 33, 1342-1344.	3.9	39
173	Analytic potential and charge model for III-V surrounding gate metal-oxide-semiconductor field-effect transistors. Journal of Applied Physics, 2012, 112, .	2.5	23
174	Multibranch Mobility Analysis for the Characterization of FDSOI Transistors. IEEE Electron Device Letters, 2012, 33, 1102-1104.	3.9	16
175	Inversion charge modeling in n-type and p-type Double-Gate MOSFETs including quantum effects: The role of crystallographic orientation. Solid-State Electronics, 2012, 67, 30-37.	1.4	7
176	Reaching sub-32nm nodes: ET-FDSOI and BOX optimization. Solid-State Electronics, 2012, 70, 101-105.	1.4	23
177	Simulation of Fabricated 20-nm Schottky Barrier MOSFETs on SOI: Impact of Barrier Lowering. IEEE Transactions on Electron Devices, 2012, 59, 1320-1327.	3.0	17
178	Two-Dimensional Monte Carlo Simulation of DGSOI MOSFET Misalignment. IEEE Transactions on Electron Devices, 2012, 59, 1621-1628.	3.0	14
179	On the effective mass of holes in inversion layers. , 2011, , .		0
180	Analytical drain current model reproducing advanced transport models in nanoscale double-gate (DG) MOSFETs. , 2011, , .		1

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181	Surface roughness scattering model for arbitrarily oriented silicon nanowires. Journal of Applied Physics, 2011, 110, 084514.	2.5	22
182	Hole effective mass in silicon inversion layers with different substrate orientations and channel directions. Journal of Applied Physics, 2011, 110, .	2.5	23
183	Ultrathin n-Channel and p-Channel SOI MOSFETs. Engineering Materials, 2011, , 169-185.	0.6	0
184	New concepts for IT-DRAMs: Overcoming the scaling limits. , 2011, , .		3
185	Properties of 22nm node extremely-thin-SOI MOSFETs. , 2011, , .		4
186	On the role of Coulomb scattering in hafnium-silicate gated silicon n and p-channel metal-oxide-semiconductor-field-effect-transistors. Journal of Applied Physics, 2011, 110, 124503.	2.5	2
187	Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32nm-node and beyond. Solid-State Electronics, 2011, 65-66, 88-93.	1.4	18
188	Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates. IEEE Transactions on Electron Devices, 2011, 58, 2371-2377.	3.0	46
189	An Inversion-Charge Analytical Model for Square Gate-All-Around MOSFETs. IEEE Transactions on Electron Devices, 2011, 58, 2854-2861.	3.0	12
190	Influence of Orientation, Geometry, and Strain on Electron Distribution in Silicon Gate-All-Around (GAA) MOSFETs. IEEE Transactions on Electron Devices, 2011, 58, 3350-3357.	3.0	14
191	In-Depth Study of Quantum Effects in SOI DGMOSFETs for Different Crystallographic Orientations. IEEE Transactions on Electron Devices, 2011, 58, 4438-4441.	3.0	6
192	Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance. Solid-State Electronics, 2011, 59, 44-49.	1.4	11
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