Francisco Gamiz

List of Publications by Year
in descending order

372	4,707	117625	168389
papers	citations	34 h-index	53 g-index

384	384	384	2486
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	On the enhanced electron mobility in strained-silicon inversion layers. Journal of Applied Physics, 2002, 92, 7320-7324.	2.5	215
2	Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion. Journal of Applied Physics, 2001, 89, 5478-5487.	2.5	142
3	Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates. Journal of Applied Physics, 2002, 92, 288-295.	2.5	141
4	Surface roughness at the Siâ€“SiO2 interfaces in fully depleted silicon-on-insulator inversion layers. Journal of Applied Physics, 1999, 86, 6854-6863.	2.5	106
5	Mechanical and thermal properties of graphene modified asphalt binders. Construction and Building Materials, 2018, 180, 265-274.	7.2	101
6	Physical model for trap-assisted inelastic tunneling in metal-oxide-semiconductor structures. Journal of Applied Physics, 2001, 90, 3396-3404.	2.5	89
7	A comprehensive model for Coulomb scattering in inversion layers. Journal of Applied Physics, 1994, 75, 924-934.	2.5	83
8	Direct and trap-assisted elastic tunneling through ultrathin gate oxides. Journal of Applied Physics, 2002, 91, 5116-5124.	2.5	77
9	Modeling the Centroid and the Inversion Charge in Cylindrical Surrounding Gate MOSFETs, Including Quantum Effects. IEEE Transactions on Electron Devices, 2008, 55, 411-416.	3.0	76
10	A Comprehensive Study of the Corner Effects in Pi-Gate MOSFETs Including Quantum Effects. IEEE Transactions on Electron Devices, 2007, 54, 3369-3377.	3.0	75
11	Monte Carlo simulation of electron transport properties in extremely thin SOI MOSFET's. IEEE Transactions on Electron Devices, 1998, 45, 1122-1126.	3.0	74
12	Acoustic phonon confinement in silicon nanolayers: Effect on electron mobility. Journal of Applied Physics, 2006, 100, 013701.	2.5	73
13	Effects of the inversion-layer centroid on the performance of double-gate MOSFETs. IEEE Transactions on Electron Devices, 2000, 47, 141-146.	3.0	72
14	Effects of the inversion layer centroid on MOSFET behavior. IEEE Transactions on Electron Devices, 1997, 44, 1915-1922.	3.0	67
15	Universality of electron mobility curves in MOSFETs: a Monte Carlo study. IEEE Transactions on Electron Devices, 1995, 42, 258-265.	3.0	62
16	An in-depth simulation study of thermal reset transitions in resistive switching memories. Journal of Applied Physics, 2013, 114, .	2.5	58
17	A simple subthreshold swing model for short channel MOSFETs. Solid-State Electronics, 2001, 45, 391-397.	1.4	56
18	A Monte Carlo study on the electronâ€transport properties of highâ€performance strainedâ€Si on relaxed Si1â^'xGexchannel MOSFETs. Journal of Applied Physics, 1996, 80, 5121-5128.	2.5	54

#	Article	IF	Citations
19	Modeling effects of electron-velocity overshoot in a MOSFET. IEEE Transactions on Electron Devices, 1997, 44, 841-846.	3.0	53
20	Role of surface-roughness scattering in double gate silicon-on-insulator inversion layers. Journal of Applied Physics, 2001, 89, 1764.	2.5	48
21	Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator. IEEE Electron Device Letters, 2012, 33, 1717-1719.	3.9	48
22	Electron mobility in extremely thin single-gate silicon-on-insulator inversion layers. Journal of Applied Physics, 1999, 86, 6269-6275.	2.5	46
23	Remote Coulomb scattering in metalâ€“oxideâ€“semiconductor field effect transistors: Screening by electrons in the gate. Applied Physics Letters, 2003, 83, 4848-4850.	3.3	46
24	Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates. IEEE Transactions on Electron Devices, 2011, 58, 2371-2377.	3.0	46
25	Reconfigurable Distributed Network Control System for Industrial Plant Automation. IEEE Transactions on Industrial Electronics, 2004, 51, 1168-1180.	7.9	45
26	Multi-Subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI. Solid-State Electronics, 2010, 54, 131-136.	1.4	43
27	A-RAM Memory Cell: Concept and Operation. IEEE Electron Device Letters, 2010, 31, 972-974.	3.9	42
28	Monte Carlo simulation of remote-Coulomb-scattering-limited mobility in metalâ€“oxideâ€“semiconductor transistors. Applied Physics Letters, 2003, 82, 3251-3253.	3.3	41
29	A Simple Approach to Quantum Confinement in Tunneling Field-Effect Transistors. IEEE Electron Device Letters, 2012, 33, 1342-1344.	3.9	39
30	Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs. IEEE Transactions on Electron Devices, 2012, 59, 3205-3211.	3.0	38
31	Assessment of field-induced quantum confinement in heterogate germanium electronâ€“hole bilayer tunnel field-effect transistor. Applied Physics Letters, 2014, 105, 082108.	3.3	38
32	A model for the quantized accumulation layer in metal-insulator-semiconductor structures. Solid-State Electronics, 1995, 38, 203-210.	1.4	37
33	Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers. Applied Physics Letters, 2006, 88, 122108.	3.3	36
34	Revisited Pseudo-MOSFET Models for the Characterization of Ultrathin SOI Wafers. IEEE Transactions on Electron Devices, 2009, 56, 1507-1515.	3.0	36
35	A review of the Z 2 -FET 1T-DRAM memory: Operation mechanisms and key parameters. Solid-State Electronics, 2018, 143, 10-19.	1.4	36
36	The dependence of the electron mobility on the longitudinal electric field in MOSFETs. Semiconductor Science and Technology, 1997, 12, 321-330.	2.0	34

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37	Scattering of electrons in silicon inversion layers by remote surface roughness. Journal of Applied Physics, 2003, 94, 392-399.	2.5	34
38	Extended Analysis of the Z^{2} -FET: Operation as Capacitorless eDRAM. IEEE Transactions on Electron Devices, 2017, 64, 4486-4491.	3.0	34
39	Modeling the equivalent oxide thickness of Surrounding Gate SOI devices with high-Î² insulators. Solid-State Electronics, 2008, 52, 1854-1860.	1.4	33
40	Why the Universal Mobility Is Not. IEEE Transactions on Electron Devices, 2010, 57, 1327-1333.	3.0	33
41	Electron mobility in double gate silicon on insulator transistors: Symmetric-gate versus asymmetric-gate configuration. Journal of Applied Physics, 2003, 94, 5732-5741.	2.5	32
42	Coulomb scattering in strainedâ€silicon inversion layers on Si1â^'xGex substrates. Applied Physics Letters, 1996, 69, 797-799.	3.3	31
43	An Analytical Iâ€“ V Model for Surrounding-Gate Transistors That Includes Quantum and Velocity Overshoot Effects. IEEE Transactions on Electron Devices, 2010, 57, 2925-2933.	3.0	30
44	Phonon-limited electron mobility in ultrathin silicon-on-insulator inversion layers. Journal of Applied Physics, 1998, 83, 4802-4806.	2.5	29
45	The Multivalley Effective Conduction Band-Edge Method for Monte Carlo Simulation of Nanoscale Structures. IEEE Transactions on Electron Devices, 2006, 53, 2703-2710.	3.0	29
46	Intra-amygdala ZIP injections impair the memory of learned active avoidance responses and attenuate conditioned taste-aversion acquisition in rats. Learning and Memory, 2011, 18, 529-533.	1.3	29
47	Metamaterial-Based Reconfigurable Intelligent Surface: 3D Meta-Atoms Controlled by Graphene Structures. IEEE Communications Magazine, 2021, 59, 42-48.	6.1	29
48	Equivalent Oxide Thickness of Trigate SOI MOSFETs With High-$kappa$ Insulators. IEEE Transactions on Electron Devices, 2009, 56, 2711-2719.	3.0	28
49	An analytical model for square GAA MOSFETs including quantum effects. Solid-State Electronics, 2010, 54, 1463-1469.	1.4	28
50	${Z}^{extsf {2}}$ -FET as Capacitor-Less eDRAM Cell For High-Density Integration. IEEE Transactions on Electron Devices, 2017, 64, 4904-4909.	3.0	28
51	Impact of Asymmetric Configurations on the Heterogate Germanium Electron–Hole Bilayer Tunnel FET Including Quantum Confinement. IEEE Transactions on Electron Devices, 2015, 62, 3560-3566.	3.0	27
52	Capacitor-less dynamic random access memory based on a IIIâ€“V transistor with a gate length of 14â€‰nm. Nature Electronics, 2019, 2, 412-419.	26.0	27
53	Effects of nonparabolic bands in quantum wires. Journal of Applied Physics, 2005, 98, 013702.	2.5	24
54	Coulomb scattering model for ultrathin silicon-on-insulator inversion layers. Applied Physics Letters, 2002, 80, 3835-3837.	3.3	23

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55	Evidence for mobility enhancement in double-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors. Journal of Applied Physics, 2007, 102, 083712.	2.5	23
56	Hole effective mass in silicon inversion layers with different substrate orientations and channel directions. Journal of Applied Physics, 2011, 110, .	2.5	23
57	Analytic potential and charge model for III-V surrounding gate metal-oxide-semiconductor field-effect transistors. Journal of Applied Physics, 2012, 112, .	2.5	23
58	Reaching sub-32nm nodes: ET-FDSOI and BOX optimization. Solid-State Electronics, 2012, 70, 101-105.	1.4	23
59	On the extension of ET-FDSOI roadmap for 22nm node and beyond. Solid-State Electronics, 2013, 90, 23-27.	1.4	23
60	Study of the effects of a stepped doping profile in short-channel MOSFETs. IEEE Transactions on Electron Devices, 1997, 44, 1425-1431.	3.0	22
61	A model for the drain current of deep submicrometer MOSFETs including electron-velocity overshoot. IEEE Transactions on Electron Devices, 1998, 45, 2249-2251.	3.0	22
62	Surface roughness scattering model for arbitrarily oriented silicon nanowires. Journal of Applied Physics, 2011, 110, 084514.	2.5	22
63	On the gate capacitance limits of nanoscale DG and FD SOI MOSFETs. IEEE Transactions on Electron Devices, 2006, 53, 753-758.	3.0	21
64	Modeling of Inversion Layer Centroid and Polysilicon Depletion Effects on Ultrathin-Gate-Oxide MOSFET Behavior: The Influence of Crystallographic Orientation. IEEE Transactions on Electron Devices, 2007, 54, 723-732.	3.0	21
65	Experimental Demonstration of Operational Z²-FET Memory Matrix. IEEE Electron Device Letters, 2018, 39, 660-663.	3.9	21
66	Hole Mobility in Ultrathin Double-Gate SOI Devices: The Effect of Acoustic Phonon Confinement. IEEE Electron Device Letters, 2009, 30, 1338-1340.	3.9	20
67	Simulation of hole mobility in two-dimensional systems. Semiconductor Science and Technology, 2009, 24, 035016.	2.0	20
68	Confinement-induced InAs/GaSb heterojunction electronâ€“hole bilayer tunneling field-effect transistor. Applied Physics Letters, 2018, 112, .	3.3	20
69	Effects of oxide-charge space correlation on electron mobility in inversion layers. Semiconductor Science and Technology, 1994, 9, 1102-1107.	2.0	19
70	A comparison of models for phonon scattering in silicon inversion layers. Journal of Applied Physics, 1995, 77, 4128-4129.	2.5	18
71	Strained-Si on Si/sub 1-x/ mosfet mobility model. IEEE Transactions on Electron Devices, 2003, 50, 1408-1411.	3.0	18
72	Hole transport in DGSOI devices: Orientation and silicon thickness effects. Solid-State Electronics, 2010, 54, 191-195.	1.4	18

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73	Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32nm-node and beyond. Solid-State Electronics, 2011, 65-66, 88-93.	1.4	18
74	Spontaneous object recognition memory in aged rats: Complexity versus similarity. Learning and Memory, 2012, 19, 444-448.	1.3	18
75	Analytical Gate Capacitance Modeling of IIIâ€“V Nanowire Transistors. IEEE Transactions on Electron Devices, 2013, 60, 1590-1599.	3.0	18
76	Experimental developments of A2RAM memory cells on SOI and bulk substrates. Solid-State Electronics, 2015, 103, 7-14.	1.4	18
77	Electron mobility in ultrathin silicon-on-insulator layers at 4.2 K. Applied Physics Letters, 2004, 84, 2298-2300.	3.3	17
78	Implications of nonparabolicity, warping, and inelastic phonon scattering on hole transport in pure Si and Ge within the effective mass framework. Journal of Applied Physics, 2005, 97, 013702.	2.5	17
79	Quantum-mechanical effects in multiple-gate MOSFETs. Journal of Computational Electronics, 2007, 6, 145-148.	2.5	17
80	Simulation of Fabricated 20-nm Schottky Barrier MOSFETs on SOI: Impact of Barrier Lowering. IEEE Transactions on Electron Devices, 2012, 59, 1320-1327.	3.0	17
81	Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation. Solid-State Electronics, 2016, 117, 60-65.	1.4	17
82	Multibranch Mobility Analysis for the Characterization of FDSOI Transistors. IEEE Electron Device Letters, 2012, 33, 1102-1104.	3.9	16
83	Electrical characterization and conductivity optimization of laser reduced graphene oxide on insulator using point-contact methods. RSC Advances, 2016, 6, 46231-46237.	3.6	16
84	Influence of the oxide-charge distribution profile on electron mobility in MOSFET's. IEEE Transactions on Electron Devices, 1995, 42, 999-1004.	3.0	15
85	Influence of mobility fluctuations on random telegraph signal amplitude in n-channel metalâ€“oxideâ€“semiconductor field-effect transistors. Journal of Applied Physics, 1997, 82, 4621-4628.	2.5	15
86	Calculation of the phonon-limited mobility in silicon Gate All-Around MOSFETs. Solid-State Electronics, 2007, 51, 1211-1215.	1.4	15
87	A new characterization technique for SOI wafers: Split C(V) in pseudo-MOSFET configuration. Solid-State Electronics, 2013, 90, 127-133.	1.4	15
88	Low-Power Z2-FET Capacitorless 1T-DRAM. , 2017, , .		15
89	An analytical expression for phononâ€limited electron mobility in siliconâ€inversion layers. Journal of Applied Physics, 1993, 74, 3289-3292.	2.5	14
90	Density of states of a twoâ€dimensional electron gas including nonparabolicity. Journal of Applied Physics, 1994, 75, 4267-4269.	2.5	14

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91	Oxide charge space correlation in inversion layers. II. Three-dimensional oxide charge distribution. Semiconductor Science and Technology, 1995, 10, 592-600.	2.0	14
92	Deep submicrometer SOI MOSFET drain current model including series resistance, self-heating and velocity overshoot effects. IEEE Electron Device Letters, 2000, 21, 239-241.	3.9	14
93	Temperature behaviour of electron mobility in double-gate silicon on insulator transistors. Semiconductor Science and Technology, 2004, 19, 113-119.	2.0	14
94	Influence of Orientation, Geometry, and Strain on Electron Distribution in Silicon Gate-All-Around (GAA) MOSFETs. IEEE Transactions on Electron Devices, 2011, 58, 3350-3357.	3.0	14
95	Two-Dimensional Monte Carlo Simulation of DGSOI MOSFET Misalignment. IEEE Transactions on Electron Devices, 2012, 59, 1621-1628.	3.0	14
96	Bias-Engineered Mobility in Advanced FD-SOI MOSFETs. IEEE Electron Device Letters, 2013, 34, 840-842.	3.9	14
97	The effect of quantum confinement on tunneling field-effect transistors with high-Î¹ gate dielectric. Applied Physics Letters, 2013, 103, .	3.3	14
98	Assessment of pseudo-bilayer structures in the heterogate germanium electron-hole bilayer tunnel field-effect transistor. Applied Physics Letters, 2015, 106, .	3.3	14
99	Analytic drain current model for IIIâ€“V cylindrical nanowire transistors. Journal of Applied Physics, 2015, 118, 044502.	2.5	14
100	Double gate silicon on insulator transistors. A Monte Carlo study. Solid-State Electronics, 2004, 48, 937-945.	1.4	13
101	Coulomb scattering in high-Î¹ gate stack silicon-on-insulator metal-oxide-semiconductor field effect transistors. Journal of Applied Physics, 2008, 104, 063704.	2.5	13
102	Influence of the interface trap location on the performance and variability of ultra-scaled MOSFETs. Microelectronics Reliability, 2013, 53, 1243-1246.	1.7	13
103	Simulation study of the electron mobility in few-layer MoS2 metalâ€“insulator-semiconductor field-effect transistors. Solid-State Electronics, 2015, 114, 30-34.	1.4	13
104	Investigating the transient response of Schottky barrier back-gated MoS₂ transistors. 2D Materials, 2020, 7, 025040.	4.4	13
105	Influence of negatively and positively charged scattering centers on electron mobility in semiconductor inversion layers: A Monte Carlo study. Journal of Applied Physics, 1995, 78, 1787-1792.	2.5	12
106	Strained-Si on Si/sub 1-x/Ge/sub x/ MOSFET inversion layer centroid modeling. IEEE Transactions on Electron Devices, 2001, 48, 2447-2449.	3.0	12
107	Effect of polysilicon depletion charge on electron mobility in ultrathin oxide MOSFETs. Semiconductor Science and Technology, 2003, 18, 927-937.	2.0	12
108	Gate bias symmetry dependency of electron mobility and prospect of velocity modulation in double-gate silicon-on-insulator transistors. Applied Physics Letters, 2004, 85, 5442-5444.	3.3	12

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109	Simulation and modelling of transport properties in strained-Si and strained-Si/SiGe-on-insulator MOSFETs. Solid-State Electronics, 2004, 48, 1347-1355.	1.4	12
110	An Inversion-Charge Analytical Model for Square Gate-All-Around MOSFETs. IEEE Transactions on Electron Devices, 2011, 58, 2854-2861.	3.0	12
111	Self-heating effects in ultrathin FD SOI transistors. , 2011, , .		12
112	Modeling the Channel Charge and Potential in Quasi-Ballistic Nanoscale Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 2640-2646.	3.0	12
113	Mobility and Capacitance Comparison in Scaled InGaAs Versus Si Trigate MOSFETs. IEEE Electron Device Letters, 2015, 36, 114-116.	3.9	12
114	Impact of the Back-Gate Biasing on Trigate MOSFET Electron Mobility. IEEE Transactions on Electron Devices, 2015, 62, 224-227.	3.0	12
115	Multisubband Ensemble Monte Carlo Analysis of Tunneling Leakage Mechanisms in Ultrascaled FDSOI, DGSOI, and FinFET Devices. IEEE Transactions on Electron Devices, 2019, 66, 1145-1152.	3.0	12
116	A procedure for the determination of the effective mobility in an N-MOSFET in the moderate inversion region. Solid-State Electronics, 1996, 39, 875-883.	1.4	11
117	A Model of the Gate Capacitance of Surrounding Gate Transistors: Comparison With Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 2477-2483.	3.0	11
118	Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance. Solid-State Electronics, 2011, 59, 44-49.	1.4	11
119	Impact of back-gate biasing on effective field and mobility in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect-transistors. Journal of Applied Physics, 2013, 113, .	2.5	11
120	A parallel deterministic solver for the SchrÃ¶dingerâ€“Poissonâ€“Boltzmann system in ultra-short DG-MOSFETs: Comparison with Monte-Carlo. Computers and Mathematics With Applications, 2014, 67, 1703-1721.	2.7	11
121	3D multi-subband ensemble Monte Carlo simulator of FinFETs and nanowire transistors. , 2014, , .		11
122	Ultra-low power 1T-DRAM in FDSOI technology. Microelectronic Engineering, 2017, 178, 245-249.	2.4	11
123	Source-to-Drain Tunneling Analysis in FDSOI, DGSOI, and FinFET Devices by Means of Multisubband Ensemble Monte Carlo. IEEE Transactions on Electron Devices, 2018, 65, 4740-4746.	3.0	11
124	Thorough Understanding of Retention Time of Z2FET Memory Operation. IEEE Transactions on Electron Devices, 2019, 66, 383-388.	3.0	11
125	Influence of the interface-state density on the electron mobility in silicon inversion layers. Journal of Electronic Materials, 1993, 22, 1159-1163.	2.2	10
126	Anisotropy of electron mobility in arbitrarily oriented FinFETs. , 2007, , .		10

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127	Monte Carlo simulation of Hall and magnetoresistance mobility in SOI devices. Solid-State Electronics, 2007, 51, 1216-1220.	1.4	10
128	Analytic Potential and Charge Model of Semiconductor Quantum Wells. IEEE Transactions on Electron Devices, 2015, 62, 4186-4191.	3.0	10
129	Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell. IEEE Electron Device Letters, 2019, 40, 1084-1087.	3.9	10
130	Random telegraph signal amplitude in submicron n-channel metal oxide semiconductor field effect transistors. Applied Physics Letters, 1997, 70, 2153-2155.	3.3	9
131	Electron transport properties of quantized silicon carbide inversion layers. Journal of Electronic Materials, 1997, 26, 203-207.	2.2	9
132	Monte Carlo simulation of electron mobility in silicon-on-insulator structures. Solid-State Electronics, 2002, 46, 1715-1721.	1.4	9
133	Modeling of retention time degradation due to inelastic trap-assisted tunneling in EEPROM devices. Microelectronics Reliability, 2003, 43, 1495-1500.	1.7	9
134	Three-interface pseudo-MOSFET models for the characterization of SOI wafers with ultrathin film and BOX. Microelectronic Engineering, 2011, 88, 1236-1239.	2.4	9
135	Compact drain-current model for reproducing advanced transport models in nanoscale double-gate MOSFETs. Semiconductor Science and Technology, 2011, 26, 095015.	2.0	9
136	Accurate Calculation of Gate Tunneling Current in Double-Gate and Single-Gate SOI MOSFETs Through Gate Dielectric Stacks. IEEE Transactions on Electron Devices, 2012, 59, 2589-2596.	3.0	9
137	Theoretical interpretation of the electron mobility behavior in InAs nanowires. Journal of Applied Physics, 2014, 116, 174505.	2.5	9
138	Implementation of Band-to-Band Tunneling Phenomena in a Multisubband Ensemble Monte Carlo Simulator: Application to Silicon TFETs. IEEE Transactions on Electron Devices, 2017, 64, 3084-3091.	3.0	9
139	MS-EMC vs. NEGF: A comparative study accounting for transport quantum corrections. , 2018, , .		9
140	InGaAs Capacitor-Less DRAM Cells TCAD Demonstration. IEEE Journal of the Electron Devices Society, 2018, 6, 884-892.	2.1	9
141	Electron velocity saturation in quantized silicon carbide inversion layers. Applied Physics Letters, 1996, 69, 2219-2221.	3.3	8
142	Electron transport in ultrathin double-gate SOI devices. Microelectronic Engineering, 2001, 59, 423-427.	2.4	8
143	An electron mobility model for ultra-thin gate-oxide MOSFETs including the contribution of remote scattering mechanisms. Semiconductor Science and Technology, 2007, 22, 348-353.	2.0	8
144	Effect of confined acoustic phonons on the electron mobility of rectangular nanowires. Applied Physics Letters, 2013, 103, .	3.3	8

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145	Multi-Subband Ensemble Monte Carlo simulation of Si nanowire MOSFETs. , 2015, , .		8
146	Competitive 1T-DRAM in 28 nm FDSOI technology for low-power embedded memory. , 2016, , .		8
147	MSDRAM, A2RAM and Z²-FET performance benchmark for 1T-DRAM applications. , 2018, , .		8
148	Gate Leakage Tunneling Impact on the InAs/GaSb Heterojunction Electronâ€“Hole Bilayer Tunneling Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4679-4686.	3.0	8
149	3-D TCAD Study of the Implications of Channel Width and Interface States on FD-SOI Z²-FETs. IEEE Transactions on Electron Devices, 2019, 66, 2513-2519.	3.0	8
150	Near-field scanning microwave microscope platform based on a coaxial cavity resonator for the characterization of semiconductor structures. Solid-State Electronics, 2019, 159, 150-156.	1.4	8
151	Simulation Perspectives of Sub-1V Single-Supply Z²-FET 1T-DRAM Cells for Low-Power. IEEE Access, 2019, 7, 40279-40284.	4.2	8
152	Electron transport in silicon-on-insulator devices. Solid-State Electronics, 2001, 45, 613-620.	1.4	7
153	A compact QM-based mobility model for nanoscale ultra-thin-body CMOS devices. , 0, , .		7
154	The effect of surface roughness scattering on hole mobility in double gate silicon-on-insulator devices. Journal of Applied Physics, 2009, 106, 023705.	2.5	7
155	Inversion charge modeling in n-type and p-type Double-Gate MOSFETs including quantum effects: The role of crystallographic orientation. Solid-State Electronics, 2012, 67, 30-37.	1.4	7
156	Switching Behavior Constraint in the Heterogate Electronâ€“Hole Bilayer Tunnel FET: The Combined Interplay Between Quantum Confinement Effects and Asymmetric Configurations. IEEE Transactions on Electron Devices, 2016, 63, 2570-2576.	3.0	7
157	2D-TCAD simulation on retention time of Z2FET for DRAM application. , 2017, , .		7
158	Evaluation of thin-oxide Z2-FET DRAM cell. , 2018, , .		7
159	Dual PN Source/Drain Reconfigurable FET for Fast and Low-Voltage Reprogrammable Logic. IEEE Access, 2020, 8, 132376-132381.	4.2	7
160	Quantum Enhancement of a S/D Tunneling Model in a 2D MS-EMC Nanodevice Simulator: NEGF Comparison and Impact of Effective Mass Variation. Micromachines, 2020, 11, 204.	2.9	7
161	Effects of bulk-impurity and interface-charge on the electron mobility in MOSFETs. Solid-State Electronics, 1995, 38, 611-614.	1.4	6
162	A theoretical interpretation of magnetoresistance mobility in silicon inversion layers. Journal of Applied Physics, 2007, 102, 013708.	2.5	6

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163	Phonon scattering in Si-based nanodevices. Solid-State Electronics, 2007, 51, 593-597.	1.4	6
164	Monte Carlo simulation of nanoelectronic devices. Journal of Computational Electronics, 2009, 8, 174-191.	2.5	6
165	In-Depth Study of Quantum Effects in SOI DGMOSFETs for Different Crystallographic Orientations. IEEE Transactions on Electron Devices, 2011, 58, 4438-4441.	3.0	6
166	Optimisation and parallelisation of a 2D MOSFET multi-subband ensemble Monte Carlo simulator. International Journal of High Performance Computing Applications, 2013, 27, 483-492.	3.7	6
167	Tunability of effective masses on MoS2 monolayers. Microelectronic Engineering, 2015, 147, 302-305.	2.4	6
168	Impact of S/D tunneling in ultrascaled devices, a Multi-Subband Ensemble Monte Carlo study. , 2015, , .		6
169	A new explicit and analytical model for square Gate-All-Around MOSFETs with rounded corners. Solid-State Electronics, 2015, 111, 180-187.	1.4	6
170	Assessment of confinement-induced band-to-band tunneling leakage in the FinEHBTFET. , 2016, , .		6
171	Simulation based DC and dynamic behaviour characterization of Z2FET. , 2017, , .		6
172	Electron trapping and detrapping in near-interfacial traps during Fowler-Nordheim tunneling injection at 77 K. Microelectronic Engineering, 1995, 28, 317-320.	2.4	5
173	Understanding the improved performance of strained channel MOSFETs. Semiconductor Science and Technology, 1997, 12, 1603-1608.	2.0	5
174	A Monte Carlo study on electron mobility in quantized cubic silicon carbide inversion layers. Journal of Applied Physics, 1997, 81, 6857-6865.	2.5	5
175	A closed-loop evaluation and validation of a method for determining the dependence of the electron mobility on the longitudinal-electric field in MOSFETs. IEEE Transactions on Electron Devices, 1997, 44, 1447-1453.	3.0	5
176	Influence of technological parameters on the behavior of the hole effective mass in SiGe structures. Journal of Applied Physics, 2000, 88, 1978-1982.	2.5	5
177	Improving strained-Si on Si/sub 1-x/Ge/sub x/ deep submicron MOSFETs performance by means of a stepped doping profile. IEEE Transactions on Electron Devices, 2001, 48, 1878-1884.	3.0	5
178	Strained-Si/SiGe-on-insulator inversion layers: The role of strained-Si layer thickness on electron mobility. Applied Physics Letters, 2002, 80, 4160-4162.	3.3	5
179	Mobility enhancement via volume inversion in double-gate MOSFETs. , 2003, , .		5
180	Remote surface roughness scattering in ultrathin-oxide MOSFETs. , 0, , .		5

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