Georges G E Gielen

List of Publications by Year
in descending order

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538 papers	10,340 citations	53794 45 h-index	74163 75 g-index
572 all docs	572 docs citations	572 times ranked	4900 citing authors

#	Article	IF	Citations
1	Improving the Accuracy of Spiking Neural Networks for Radar Gesture Recognition Through Preprocessing. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 2869-2881.	11.3	10
2	A Compact, Low-Power Analog Front-End With Event-Driven Input Biasing for High-Density Neural Recording in 22-nm FDSOI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 804-808.	3.0	10
3	Fail-Safe Human Detection for Drones Using a Multi-Modal Curriculum Learning Approach. IEEE Robotics and Automation Letters, 2022, 7, 303-310.	5.1	6
4	Methodology for Readout and Ring Oscillator Optimization Toward Energy-Efficient VCO-Based ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 985-998.	5.4	5
5	On the Use of Spiking Neural Networks for Ultralow-Power Radar Gesture Recognition. IEEE Microwave and Wireless Components Letters, 2022, 32, 222-225.	3.2	8
6	A 256-Channel Actively-Multiplexed ÂµECoG Implant with Column-Parallel Incremental $DeltaSigma$ ADCs Employing Bulk-DACs in 22-nm FDSOI Technology. , 2022, , .		4
7	A 96.9-dB-Resolution 109-Î¼W Second-Order Robust Closed-Loop VCO-Based Sensor Interface for Multiplexed Single-Ended Resistance Readout in 180-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 2764-2777.	5.4	4
8	Exploring Cross-fusion and Curriculum Learning for Multi-modal Human Detection on Drones. , 2022, , .		0
9	A Low-Complexity Radar Detector Outperforming OS-CFAR for Indoor Drone Obstacle Avoidance. IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing, 2021, 14, 9162-9175.	4.9	20
10	Analysis and Comparison of Readout Architectures and Analog-to-Digital Converters for 3D-Stacked CMOS Image Sensors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3117-3130.	5.4	9
11	Power-efficient VCO-based ADCs for Wireless Communication Systems. , 2021, , .		0
12	Efficient Offline Outer/Inner DAC Mismatch Calibration in Wideband Î”Î£ ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4259-4269.	5.4	1
13	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS?Part 2: Architectures and Circuits. IEEE Solid-State Circuits Magazine, 2020, 12, 18-27.	0.4	15
14	A 16.1-bit Resolution 0.064-mm² Compact Highly Digital Closed-Loop Single-VCO-Based 1-1 Sturdy-MASH Resistance-to-Digital Converter With High Robustness in 180-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 2456-2467.	5.4	17
15	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS-Part 1: Basic Principles. IEEE Solid-State Circuits Magazine, 2020, 12, 47-55.	0.4	41
16	Improving the EMI Robustness of Feedback-based Time-Encoding Readout Architectures for Resistive Sensor Interfaces. , 2020, , .		2
17	Machine Learning-based Defect Coverage Boosting of Analog Circuits under Measurement Variations. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-27.	2.6	4
18	Quick Analyses for Improving Reliability and Functional Safety of Mixed-Signal ICs. , 2020, , .		1

#	Article	IF	Citations
19	Review of Methodologies for Pre- and Post-Silicon Analog Verification in Mixed-Signal SOCs. , 2019, , .		8
20	Introduction to the Special Issue on the 2019 IEEE European Solid-State Circuits Conference (ESSCIRC). IEEE Solid-State Circuits Letters, 2019, 2, 61-62.	2.0	0
21	From Open-Loop to Closed-Loop Single-VCO-Based Sensor-to-Digital Converter Architectures: theoretical analysis and comparison. , 2019, , .		6
22	Architectural Analysis of a Novel Closed-Loop VCO-Based 1â€“1 Sturdy MASH Sensor-to-Digital Converter. , 2019, , .		1
23	A Robust BBPLL-Based 0.18-mu m CMOS Resistive Sensor Interface With High Drift Resilience Over a â^’40 Â°Câ€“175 Â°C Temperature Range. IEEE Journal of Solid-State Circuits, 2019, 54, 1862-1873.	5.4	15
24	An 85-MHz-BW ASAR-Assisted CT 4-0 MASH $DeltaSigma$ Modulator With Background Half-Range Dithering-Based DAC Calibration in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2405-2414.	5.4	7
25	Applying Vstress and defect activation coverage to produce zero-defect mixed-signal automotive ICs. , 2019, , .		9
26	The fantastic voyage towards ultra-miniaturized sensing circuits. , 2019, , .		0
27	Performance Limitation Analysis of Highly-Digital Time-Based Closed-Loop Sensor-to-Digital Converter Architectures. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1114-1118.	3.0	5
28	Understanding the Impact of Time-Dependent Random Variability on Analog ICs: From Single Transistor Measurements to Circuit Simulations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 601-610.	3.1	18
29	A 16.1-b ENOB 0.064mm2 Compact Highly-Digital Closed-Loop Single-VCO-based 1â€“1 SMASH Resistance-to-Digital Converter in 180nm CMOS. , 2019, , .		1
30	ADAGE: Automatic DfT-Assisted Generation of Test Stimuli for Mixed- Signal Integrated Circuits. IEEE Design and Test, 2018, 35, 24-30.	1.2	4
31	A 0.18- $mu ext{m}$ CMOS Image Sensor With Phase-Delay-Counting and Oversampling Dual-Slope Integrating Column ADCs Achieving $1{ext {e}}^{-}_{mathrm{ rms}}$ Noise at 3.8- $mu ext{s}$ Conversion Time. IEEE Journal of Solid-State Circuits, 2018, 53, 515-526.	5.4	4
32	Methodology Towards Sub-ppm Testing of Analog and Mixed-Signal ICs for Cyber-Physical Systems. , 2018, , .		1
33	An Automated Low-Cost Analog and Mixed-Signal DfT Method Using Testing Diodes. IEEE Design and Test, 2018, 35, 15-23.	1.2	0
34	A/D Converters and Applications. Signals and Communication Technology, 2018, , 13-35.	0.5	0
35	Continuous-Time Delta-Sigma Modulators. Signals and Communication Technology, 2018, , 37-66.	0.5	0
36	VCO-Based ADCs. Signals and Communication Technology, 2018, , 67-81.	0.5	0

#	Article	IF	Citations
37	CT DSM ADCs with VCO-Based Quantization. Signals and Communication Technology, 2018, , 83-108.	0.5	0
38	VCO-Based 0- $$varDelta varSigma $$ MASH ADC. Signals and Communication Technology, 2018, , 127-151.	0.5	0
39	Fully-VCO-Based High-Order $$varDelta varSigma $$ ADC. Signals and Communication Technology, 2018, , 153-171.	0.5	0
40	Improving the robustness and drift resilience of CMOS BBPLL-based time-based sensor interfaces. , 2018, , .		0
41	A Single-Temperature-Calibration 0.18-Âµm CMOS Time-Based Resistive Sensor Interface with Low Drift over a â^'40Â°C to 175Â°C Temperature Range. , 2018, , .		5
42	Controlled-Oscillator Optimization for Highly-Digital CMOS Time-Based Sensor-to-Digital Converter Architectures. , 2018, , .		2
43	Generalized mode solver for plasmonic transmission lines embedded in layered media based on the Method of Moments. Computer Physics Communications, 2018, 233, 1-15.	7.5	3
44	Fullyâ€VCOâ€based 0â€2ÂMASH CT Î”Î£ ADC. Electronics Letters, 2018, 54, 1018-1020.	1.0	6
45	Modeling and Analysis of Drift-Cancellation Techniques for Time-Based Integrated Resistive Sensor Interfaces. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1203-1212.	2.5	4
46	Design of Power-Efficient Highly Digital Analog-to-Digital Converters for Next-Generation Wireless Communication Systems. Signals and Communication Technology, 2018, , .	0.5	2
47	Low-Noise Detectors through Incremental Sigmaâ€“Delta ADCs. , 2017, , 71-90.		0
48	A Review on Internet of Things Solutions for Intelligent Energy Control in Buildings for Smart City Applications. Energy Procedia, 2017, 111, 770-779.	1.8	147
49	Novel Wire-Grid Nano-Antenna Array With Circularly Polarized Radiation for Wireless Optical Communication Systems. Journal of Lightwave Technology, 2017, 35, 4700-4706.	4.6	14
50	Analysis and modeling of drift-resilient time-based integrated resistive sensor interfaces. , 2017, , .		3
51	Drift mitigation in integrated sensor interfaces. , 2017, , .		0
52	A fully-integrated method for RTN parameter extraction. , 2017, , .		3
53	A very low cost and highly parallel DfT method for analog and mixed-signal circuits. , 2017, , .		6
54	A 0.6-V, 0.015-mm², Time-Based ECG Readout for Ambulatory Applications in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 298-308.	5.4	44

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55	A 5Gb/s 7.1fJ/b/mm 8Ã— multi-drop on-chip 10mm data link in 14nm FinFET CMOS SOI at 0.5V. , 2017, , .		1
56	A power-efficient reconfigurable two-step VCO-based ADC for software-defined radio. , 2017, , .		0
57	Automatic testing of analog ICs for latent defects using topology modification. , 2017, , .		11
58	Non-intrusive detection of defects in mixed-signal integrated circuits using light activation. , 2017, , .		1
59	Spherical Wave Based Macromodels for Efficient System-Level EMC Analysis in Circuit Simulators Part II: Optimized Calculation of DUTâ€“DUT Interactions. IEEE Transactions on Electromagnetic Compatibility, 2016, 58, 1506-1516.	2.2	1
60	A surrogate model assisted evolutionary algorithm for computationally expensive design optimization problems with discrete variables. , 2016, , .		8
61	Comparative experimental analysis of time-dependent variability using a transistor test array. , 2016, , .		7
62	Analog fault coverage improvement using final-test dynamic part average testing. , 2016, , .		16
63	Effective DC fault models and testing approach for open defects in analog circuits. , 2016, , .		19
64	Automatic test signal generation for mixed-signal integrated circuits using circuit partitioning and interval analysis. , 2016, , .		5
65	Automatic generation of test infrastructures for analog integrated circuits by controllability and observability co-optimization. The Integration VLSI Journal, 2016, 55, 393-400.	2.1	10
66	Magnetic hysteresis at the domain scale of a multi-scale material model for magneto-elastic behaviour. Journal of Magnetism and Magnetic Materials, 2016, 414, 168-179.	2.3	23
67	Digital-domain chopping technique for high-resolution PLL-based sensor interfaces. Sensors and Actuators A: Physical, 2016, 249, 294-302.	4.1	11
68	Charge pumpâ€•and VCOâ€‘based secondâ€•order deltaâ€‘sigma ADC. Electronics Letters, 2016, 52, 1432-1434.	1.0	2
69	An integrated multi-electrode-optrode array for in vitro optogenetics. Scientific Reports, 2016, 6, 20353.	3.3	36
70	Low Loss CMOS-Compatible PECVD Silicon Nitride Waveguides and Grating Couplers for Blue Light Optogenetic Applications. IEEE Photonics Journal, 2016, 8, 1-11.	2.0	29
71	A column-and-row-parallel CMOS image sensor with thermal and 1/f noise suppression techniques. , 2016, , .		3
72	Spherical Wave Based Macromodels for Efficient System-Level EMC Analysis in Circuit Simulators Part I: Optimized Derivation and Truncation Criteria. IEEE Transactions on Electromagnetic Compatibility, 2016, 58, 1494-1505.	2.2	3

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73	Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 577-586.	5.4	20
74	A Surrogate-Model-Assisted Evolutionary Algorithm for Computationally Expensive Design Optimization Problems with Inequality Constraints. Springer Proceedings in Mathematics and Statistics, 2016, , 347-370.	0.2	9
75	Digital-domain Chopping Technique for PLL-Based Sensor Interfaces. Procedia Engineering, 2015, 120, 507-510.	1.2	1
76	High-density optrode-electrode neural probe using SixNy photonics for in vivo optogenetics. , 2015, , .		15
77	A lowpass/bandpass reconfigurable continuous-time Î”Î£ ADC for software-defined radio. , 2015, , .		0
78	Towards Energy-Efficient CMOS Integrated Sensor-to-Digital Interface Circuits. , 2015, , 379-397.		2
79	Automatic generation of autonomous built-in observability structures for analog circuits. , 2015, , .		7
80	Grain scale hysteresis model embedded in a multi-scale material model. , 2015, , .		2
81	Embedding a Magnetoelastic Material Model in a Coupled Magnetomechanical Finite-Element Solver. IEEE Transactions on Magnetics, 2015, 51, 1-4.	2.1	4
82	Automatic generation of lightweight controllability and observability structures for analog circuits. , 2015, , .		3
83	A 42 fJ/Step-FoM Two-Step VCO-Based Delta-Sigma ADC in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 714-723.	5.4	61
84	Development of an Ultralow-Power Injection-Locked PSK Receiver Architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 31-35.	3.0	2
85	Automated testing of mixed-signal integrated circuits by topology modification. , 2015, , .		16
86	Impact analysis of deep-submicron CMOS technologies on the voltage and temperature independence of a time-domain sensor interface. Analog Integrated Circuits and Signal Processing, 2015, 82, 285-296.	1.4	1
87	A 40ÂMHz-BW 12-bit continuous-time âˆ†Î£ modulator with digital calibration and 84.2ÂdB-SFDR in 90Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2015, 84, 137-148.	1.4	0
88	A presence-based control strategy solution for HVAC systems. , 2015, , .		5
89	Design of low-power sensor interfaces in the IoT era. , 2015, , .		1
90	A 40-MHz Bandwidth 0â€“2 MASH VCO-Based Delta-Sigma ADC With 35-fJ/Step FoM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 952-956.	3.0	22

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91	Time-based sensor interface circuits in carbon nanotube technology. , 2015, , .		1
92	Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks. Analog Circuits and Signal Processing Series, 2015, , .	0.3	5
93	A Low-Energy Ultra-Wideband Internet-of-Things Radio System for Multi-Standard Smart-Home Energy Management. IEIE Transactions on Smart Processing and Computing, 2015, 4, 354-365.	0.4	6
94	SMAS: A Generalized and Efficient Framework for Computationally Expensive Electronic Design Optimization Problems. , 2015, , 251-275.		1
95	Behavioral study of the surrogate model-aware evolutionary search framework. , 2014, , .		18
96	Network on Chip optimization based on surrogate model assisted evolutionary algorithms. , 2014, , .		5
97	An Integrated a-IGZO UHF Energy Harvester for Passive RFID Tags. IEEE Transactions on Electron Devices, 2014, 61, 3289-3295.	3.0	44
98	Design and test of analog circuits towards sub-ppm level. , 2014, , .		19
99	“All Programmable SOC FPGA for networking and computing in big data infrastructure”. , 2014, , .		2
100	Design and implementation of a multi-standard event-driven energy management system for smart buildings. , 2014, , .		3
101	Integral equations formulation of plasmonic transmission lines. Optics Express, 2014, 22, 22388.	3.4	21
102	Finiteâ€element discretisation of the eddyâ€current term in a 2D solver for radially symmetric models. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2014, 27, 505-516.	1.9	4
103	Fundamentals of Optimization Techniques in Analog IC Sizing. Studies in Computational Intelligence, 2014, , 19-40.	0.9	3
104	Automatic generation of electro-thermal models with TRAPPIST. , 2014, , .		0
105	0.35 V timeâ€domainâ€based instrumentation amplifier. Electronics Letters, 2014, 50, 1511-1513.	1.0	5
106	A fully micromachined double-slot waveguide-to-GCPW transition for 180–230 GHz MM-wave applications. , 2014, , .		3
107	A 40MHz-BW 35fJ/step-FoM nonlinearity-cancelling two-step ADC with dual-input VCO-based quantizer. , 2014, , .		8
108	Automated Design of Analog and High-frequency Circuits. Studies in Computational Intelligence, 2014, , .	0.9	31

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109	Electromagnetic Design Automation: Surrogate Model Assisted Evolutionary Algorithm. Studies in Computational Intelligence, 2014, , 133-151.	0.9	0
110	Efficient optimization of fully-integrated inductive DCâ€“DC converters comprising tapered inductor layout synthesis and temperature effects. Analog Integrated Circuits and Signal Processing, 2014, 78, 111-121.	1.4	1
111	A Gaussian Process Surrogate Model Assisted Evolutionary Algorithm for Medium Scale Expensive Optimization Problems. IEEE Transactions on Evolutionary Computation, 2014, 18, 180-192.	10.0	379
112	Sparse $$varepsilon $$ Îµ -tube support vector regression by active learning. Soft Computing, 2014, 18, 1113-1126.	3.6	6
113	Deep-level transient spectroscopy on an amorphous InGaZnO₄ Schottky diode. Applied Physics Letters, 2014, 104, 082112.	3.3	24
114	Nonlinear Magnetostatic Finite-Element Formulation for Models With Radial Symmetry. IEEE Transactions on Magnetics, 2014, 50, 85-88.	2.1	3
115	Two-Dimensional Magnetostatic Finite-Element Simulation for Devices With a Radial Symmetry. IEEE Transactions on Magnetics, 2014, 50, 1-4.	2.1	10
116	An Efficient Method for Antenna Design Optimization Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Antennas and Propagation, 2014, 62, 7-18.	5.1	194
117	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	5.4	101
118	Stochastic Macromodeling of Nonlinear Systems Via Polynomial Chaos Expansion and Transfer Function Trajectories. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 1454-1460.	4.6	23
119	An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe. IEEE Journal of Solid-State Circuits, 2014, 49, 248-261.	5.4	208
120	Optimization of analog fault coverage by exploiting defect-specific masking. , 2014, , .		16
121	High-Performance a-IGZO Thin Film Diode as Selector for Cross-Point Memory Application. IEEE Electron Device Letters, 2014, 35, 642-644.	3.9	39
122	A Low-Noise High-Frame-Rate 1-D Decoding Readout Architecture for Stacked Image Sensors. IEEE Sensors Journal, 2014, 14, 1966-1973.	4.7	5
123	Low-energy UWB transceiver implementation for smart home energy management. , 2014, , .		7
124	PTC-Based Sigma-Delta ADCs for High-Speed, Low-Noise Imagers. IEEE Sensors Journal, 2014, 14, 2932-2933.	4.7	7
125	Design of a frequency reference based on a PVT-independent transmission line delay. , 2014, , .		0
126	Scalable Bangâ€“Bang Phase-Locked-Loop-based integrated sensor interfaces. Microelectronics Journal, 2014, 45, 1641-1647.	2.0	4

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127	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	14.6	70
128	A remotely-powered, 20ÂMb/s, 5.35ÂpJ/bit impulse-UWB WSN tag for cm-accurate-localization sensor networks. Analog Integrated Circuits and Signal Processing, 2014, 80, 531-540.	1.4	1
129	GASPAD: A General and Efficient mm-Wave Integrated Circuit Synthesis Method Based on Surrogate Model Assisted Evolutionary Algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 169-182.	2.7	79
130	A 132-dB Dynamic-Range Global-Shutter Stacked Architecture for High-Performance Imagers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 398-402.	3.0	8
131	Transient Behavior and Phase Noise Performance of Pulsed-Harmonic Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2119-2128.	5.4	2
132	Closed-loop optical neural stimulation based on a 32-channel low-noise recording system with online spike sorting. Journal of Neural Engineering, 2014, 11, 046005.	3.5	43
133	Basic Concepts and Background. Studies in Computational Intelligence, 2014, , 1-17.	0.9	2
134	Process Variation-Aware Analog Circuit Sizing: Uncertain Optimization. Studies in Computational Intelligence, 2014, , 85-105.	0.9	0
135	Ordinal Optimization-Based Methods for Efficient Variation-Aware Analog IC Sizing. Studies in Computational Intelligence, 2014, , 107-131.	0.9	0
136	High-Performance Analog IC Sizing: Advanced Constraint Handling and Search Methods. Studies in Computational Intelligence, 2014, , 41-62.	0.9	0
137	Mixed-signal template-based reduction scheme for stimulus artifact removal in electrical stimulation. Medical and Biological Engineering and Computing, 2013, 51, 449-458.	2.8	1
138	Miniaturization of UWB Antennas and its Influence on Antenna-Transceiver Performance in Impulse-UWB Communication. Wireless Personal Communications, 2013, 71, 2913-2935.	2.7	2
139	An Efficient Evolutionary Algorithm for Chance-Constrained Bi-Objective Stochastic Optimization. IEEE Transactions on Evolutionary Computation, 2013, 17, 786-796.	10.0	43
140	Black-Box Modelling of AC-DC Rectifiers for RFID Applications Using Support Vector Regression Machines. , 2013, , .		2
141	An energy-efficient capacitance-controlled oscillator-based sensor interface for MEMS sensors. , 2013, , .		13
142	Extracting Analytical Nonlinear Models from Analog Circuits by Recursive Vector Fitting of Transfer Function Trajectories. , 2013, , .		6
143	Timing-based integrated sensor interfaces: Hype or promise?. , 2013, , .		0
144	A 40MHz-BW two-step open-loop VCO-based ADC with 42fJ/step FoM in 40nm CMOS. , 2013, , .		7

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145	A 40nm-CMOS, 72 µW injection-locked timing reference and 1.8 Mbit/s coordination receiver for wireless sensor networks. , 2013, , .		0
146	Developing engineering-oriented educational workshops within a student branch. , 2013, , .		0
147	Calibration of DAC Mismatch Errors in $SigmaDelta$ ADCs Based on a Sine-Wave Measurement. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 567-571.	3.0	30
148	Gigahertz Operation of a-IGZO Schottky Diodes. IEEE Transactions on Electron Devices, 2013, 60, 3407-3412.	3.0	64
149	Stochastic Degradation Modeling and Simulation for Analog Integrated Circuits in Nanometer CMOS. , 2013, , .		9
150	A 40nm-CMOS, 18 μW, temperature and supply voltage independent sensor interface for RFID tags. , 2013, , .		7
151	Experimental demonstration of a fully digital capacitive sensor interface built entirely using carbon-nanotube FETs. , 2013, , .		18
152	Performance Analysis of Energy-Efficient BBPLL-Based Sensor-to-Digital Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2130-2138.	5.4	18
153	Efficient Reciprocity-Based Algorithm to Predict Worst Case Induced Disturbances on Multiconductor Transmission Lines due to Incoming Plane Waves. IEEE Transactions on Electromagnetic Compatibility, 2013, 55, 208-216.	2.2	42
154	Supply-Noise-Resilient Design of a BBPLL-Based Force-Balanced Wheatstone Bridge Interface in 130-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2618-2627.	5.4	52
155	A Gain-Adaptive Column Amplifier for Wide-Dynamic-Range CMOS Image Sensors. IEEE Transactions on Electron Devices, 2013, 60, 3601-3604.	3.0	2
156	Impact of transistor aging on RF low noise amplifier performance of 28nm technology: Reliability assessment. , 2013, , .		8
157	A Low-Power and Low-Voltage BBPLL-Based Sensor Interface in 130nm CMOS for Wireless Sensor Networks. , 2013, , .		2
158	Sacha. , 2013, , .		8
159	40ÂMHzâ€BW continuousâ€time Î”Î£ modulator with capacitive local feedback and currentâ€sharing OTA. Electronics Letters, 2013, 49, 585-587.	1.0	2
160	Development of an open-source smart energy house for K-12 education. , 2013, , .		3
161	Integrated UHF a-IGZO energy harvester for passive RFID tags. , 2013, , .		12
162	An implantable 455-active-electrode 52-channel CMOS neural probe. , 2013, , .		30

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163	Efficient Synthesis Methods for High-Frequency Integrated Passive Components and Amplifiers. Lecture Notes in Electrical Engineering, 2013, , 27-52.	0.4	0
164	Predictive sensing in analog-to-digital converters for biomedical applications. , 2013, , .		0
165	A third-order complementary metalâ€“oxideâ€“semiconductor sigma-delta modulator operating between 4.2 K and 300 K. Review of Scientific Instruments, 2012, 83, 024708.	1.3	5
166	Wobble-based on-chip calibration circuit for temperature independent oscillators. Electronics Letters, 2012, 48, 1000-1001.	1.0	2
167	Efficient multi-objective synthesis for microwave components based on computational intelligence techniques. , 2012, , .		9
168	Impact of TSV area on the dynamic range and frame rate performance of 3D-integrated image sensors. , 2012, , .		2
169	UHF IGZO Schottky diode. , 2012, , .		21
170	Black-box modelling of conducted electromagnetic immunity by support vector machines. , 2012, , .		2
171	Towards a noise prediction model for in vivo neural recording. , 2012, 2012, 759-62.		13
172	Black-box modelling of conducted electromagnetic emissions by adjustable complexity support vector regression machines. , 2012, , .		1
173	High-performance a-In-Ga-Zn-O Schottky diode with oxygen-treated metal contacts. Applied Physics Letters, 2012, 101, .	3.3	81
174	An Efficient High-Frequency Linear RF Amplifier Synthesis Method Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 981-993.	2.7	53
175	Degradation-Resilient Design of a Self-Healing xDSL Line Driver in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 1757-1767.	5.4	9
176	Complementary DAC topology for reduced output impedance dependency and improved dynamic performance. Electronics Letters, 2012, 48, 1039-1041.	1.0	9
177	A Novel, Highly Linear, Voltage and Temperature Independent Sensor Interface using Pulse Width Modulation. Procedia Engineering, 2012, 47, 1215-1218.	1.2	8
178	A 127 μW exact timing reference for Wireless Sensor Networks based on injection locking. , 2012, , .		2
179	Offset measurement method for accurate characterization of BTI-induced degradation in opamps. , 2012, , .		2
180	Optimization of fully-integrated power converter circuits comprising tapered inductor layout and temperature effects. , 2012, , .		3

#	Article	IF	Citations
181	Designing reliable analog circuits in an unreliable world. , 2012, , .		14
182	Miniaturized RFID/UWB Antenna Structure that Can be Optimized for Arbitrary Input Impedance. IEEE Antennas and Propagation Magazine, 2012, 54, 74-87.	1.4	5
183	Characterization of Analog Circuits Using Transfer Function Trajectories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1796-1804.	5.4	17
184	Miniaturized integrated antennas for far-field wireless powering. AEU - International Journal of Electronics and Communications, 2012, 66, 789-796.	2.9	3
185	Design of an intrinsically-linear double-VCO-based ADC with 2nd-order noise shaping. , 2012, , .		1
186	Advances in variation-aware modeling, verification, and testing of analog ICs. , 2012, , .		8
187	A fast analog circuit yield estimation method for medium and high dimensional problems. , 2012, , .		4
188	Capacitance-Controlled Oscillator with Enhanced Tuning Range using Negative Capacitance for Time-Based Sensor Interfaces. Procedia Engineering, 2012, 47, 21-24.	1.2	3
189	An Ultra-Low-Power, Batteryless Microsystem for Wireless Sensor Networks. Procedia Engineering, 2012, 47, 1406-1409.	1.2	1
190	Dynamic Offset Cancellation for PLL-Based Sensor Interfaces. Procedia Engineering, 2012, 47, 1319-1322.	1.2	3
191	Self-adaptive lower confidence bound: A new general and effective prescreening method for Gaussian Process surrogate model assisted evolutionary algorithms. , 2012, , .		6
192	Hierarchical analog circuit reliability analysis using multivariate nonlinear regression and active learning sample selection. , 2012, , .		16
193	Fully micromachined W-band rectangular waveguide to grounded coplanar waveguide transition. IET Microwaves, Antennas and Propagation, 2012, 6, 533.	1.4	8
194	A selectable-bandwidth 3.5 mW, 0.03Âmm2 self-oscillating Sigma Delta modulator with 71 dB dynamic range at 5ÂMHz and 65 dB at 10ÂMHz bandwidth. Analog Integrated Circuits and Signal Processing, 2012, 72, 55-63.	1.4	3
195	Sparse multikernel support vector regression machines trained by active learning. Expert Systems With Applications, 2012, 39, 11029-11035.	7.6	12
196	Recurrent sparse support vector regression machines trained by active learning in the time-domain. Expert Systems With Applications, 2012, 39, 10933-10942.	7.6	16
197	A Multichannel Integrated Circuit for Electrical Recording of Neural Activity, With Independent Channel Programmability. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 101-110.	4.0	66
198	A 40MHz 12bit 84.2dB-SFDR continuous-time delta-sigma modulator in 90nm CMOS. , 2011, , .		6

#	Article	IF	Citations
199	Analysis of the doubled-slot end-wall waveguide to CPW transition. , 2011, , .		4
200	A fully-digital, 0.3V, 270 nW capacitive sensor interface without external references. , 2011, , .		46
201	A 0.6V to 1.6V, 46μW voltage and temperature independent 48 MHz pulsed LC oscillator for RFID tags. , 2011, , .		3
202	Transistor aging-induced degradation of analog circuits: Impact analysis and design guidelines. , 2011, , .		37
203	An automated calibration system for in vivo neural network study. , 2011, , .		0
204	Efficient analytical macromodeling of large analog circuits by Transfer Function Trajectories. , 2011, , .		4
205	A failure-resilient xDSL line driver with on-chip degradation monitor. , 2011, , .		2
206	A compact NBTI model for accurate analog integrated circuit reliability simulation. , 2011, , .		12
207	A Rigorous Approach to the Robust Design of Continuous-Time $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2829-2837.	5.4	11
208	Capacitance-controlled oscillator optimization for integrated capacitive sensors with time/frequency-based conversion. Procedia Engineering, 2011, 25, 1301-1304.	1.2	6
209	An Enhanced, Highly Linear, Fully-Differential PLL- Based Sensor Interface. Procedia Engineering, 2011, 25, 1597-1600.	1.2	5
210	UWB signal acquisition in transmit-only networks. , 2011, , .		1
211	Miniaturised integrated antenna set for RFID/UWB applications. Electronics Letters, 2011, 47, 82.	1.0	2
212	Computer-Aided Analog Circuit Design for Reliability in Nanometer CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 50-58.	3.6	65
213	Lighting the Way. IEEE Solid-State Circuits Magazine, 2011, 3, 27-34.	0.4	0
214	A novel, PLL-based frequency-to-digital conversion mechanism for sensor interfaces. Sensors and Actuators A: Physical, 2011, 172, 220-227.	4.1	22
215	Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 793-805.	2.7	93
216	Synthesis of Integrated Passive Components for High-Frequency RF ICs Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1458-1468.	2.7	63

#	Article	IF	Citations
217	A Volterra Series Nonlinear Model of the Sampling Distortion in Flash ADCs Due to Substrate Noise Coupling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 877-881.	3.0	10
218	Trustworthy Genetic Programming-Based Synthesis of Analog Circuit Topologies Using Hierarchical Domain-Specific Building Blocks. IEEE Transactions on Evolutionary Computation, 2011, 15, 557-570.	10.0	45
219	Effect of temperature on phosphorus sorption to sediments from shallow eutrophic lakes. Ecological Engineering, 2011, 37, 1515-1522.	3.6	59
220	Impact analysis of stochastic transistor aging on current-steering DACs in 32nm CMOS. , 2011, , .		1
221	Systematic design of a programmable low-noise CMOS neural interface for cell activity recording. , 2011, , .		2
222	A 16-channel low-noise programmable system for the recording of neural signals. , 2011, , .		2
223	A novel operating-point driven method for the sizing of analog IC. , 2011, , .		4
224	Analog circuit reliability in sub-32 nanometer CMOS: Analysis and mitigation. , 2011, , .		28
225	Stochastic circuit reliability analysis. , 2011, , .		13
226	4+1-transistor pixel architecture for high-speed, high-resolution CMOS image sensors. Electronics Letters, 2011, 47, 1221.	1.0	1
227	Mitigation of sampling distortion in regenerative comparators by passive source degeneration. Electronics Letters, 2011, 47, 645.	1.0	0
228	Analyzing and modeling the performance degradation of flash A/D converters due to substrate noise coupling. Analog Integrated Circuits and Signal Processing, 2010, 65, 185-195.	1.4	2
229	A novel PLL-based sensor interface for resistive pressure sensors. Procedia Engineering, 2010, 5, 62-65.	1.2	4
230	Design automation towards reliable analog integrated circuits. , 2010, , .		7
231	A 0.5 V-1.4 V supply-independent frequency-based analog-to-digital converter with fast start-up time for wireless sensor networks. , 2010, , .		5
232	Towards a closed-loop system for stimulation and recording: An in vitro approach with embryonic cardiomyocytes. , 2010, 2010, 2735-8.		1
233	Sizing mixed-mode circuits by multi-objective evolutionary algorithms. , 2010, , .		2
234	A cryogenic analog to digital converter operating from 300 K down to 4.4 K. Review of Scientific Instruments, 2010, 81, 024702.	1.3	29

#	Article	IF	Citations
235	Variability-aware reliability simulation of mixed-signal ICs with quasi-linear complexity. , 2010, , .		11
236	Efficient simulation model for DAC dynamic properties. , 2010, , .		2
237	An enhanced MOEA/D-DE and its application to multiobjective analog cell sizing. , 2010, , .		29
238	Compact trajectory-based behavioural models for analogue circuits. Electronics Letters, 2010, 46, 1058.	1.0	4
239	Interleaved data weighted averaging technique for speed/power relaxation in multi-bit DACs. Electronics Letters, 2010, 46, 32.	1.0	1
240	Far-field RF powering system for RFID and implantable devices with monolithically integrated on-chip antenna. , 2010, , .		20
241	Far-Field On-Chip Antennas Monolithically Integrated in a Wireless-Powered 5.8-GHz Downlink/UWB Uplink RFID Tag in 0.18-$mu{hbox {m}}$ Standard CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1746-1758.	5.4	67
242	A Reconfigurable, 130 nm CMOS 108 pJ/pulse, Fully Integrated IR-UWB Receiver for Communication and Precise Ranging. IEEE Journal of Solid-State Circuits, 2010, 45, 69-83.	5.4	48
243	Energy Normalized Correlation for Signal Acquisition in Power-Control-Absent UWB Networks. IEEE Communications Letters, 2010, 14, 653-655.	4.1	1
244	Efficient Variability-Aware NBTI and Hot Carrier Circuit Reliability Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1884-1893.	2.7	36
245	NBTI model for analogue IC reliability simulation. Electronics Letters, 2010, 46, 1279.	1.0	14
246	A Monolithically Integrated On-Chip Antenna in 0.18 <formula formulatype="inline"> <tex Notation="TeX">mu</tex> </formula>m Standard CMOS Technology for Far-Field Short-Range Wireless Powering. IEEE Antennas and Wireless Propagation Letters, 2010, 9, 631-633.	4.0	15
247	A 2.8-to-8.5mW GSM/bluetooth/UMTS/DVB-H/WLAN fully reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G radios in 90nm digital CMOS. , 2010, , .		22
248	Fully integrated 1.2 pJ/p UWB transmitter with on-chip antenna for wireless identification. , 2010, , .		5
249	A volterra series-enhanced model to predict the non-linear sampling distortion in flash A/D converters due to substrate noise. , 2010, , .		0
250	An accurate and efficient yield optimization method for analog circuits based on computing budget allocation and memetic search technique. , 2010, , .		3
251	The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 416-420.	3.0	13
252	Towards automated extraction of EMC-aware trajectory-based macromodels for analog circuits. , 2009, , .		0

#	Article	IF	Citations
253	Decomposition-based multi-objective optimization of second-generation current conveyors. , 2009, , .		9
254	Optimizing current conveyors by evolutionary algorithms including differential evolution. , 2009, , .		17
255	Health-care electronics The market, the challenges, the progress. , 2009, , .		0
256	A design methodology for fully reconfigurable Delta-Sigma data converters. , 2009, , .		0
257	Modeling the impact of local and distant electrode configuration on the stimulation pattern in micrometer-size neural probes. , 2009, , .		0
258	Efficient reliability simulation of analog ICs including variability and time-varying stress. , 2009, , .		21
259	Massively multi-topology sizing of analog integrated circuits. , 2009, , .		19
260	Prediction of non-uniform sampling distortion due to substrate noise coupling in regenerative comparators. , 2009, , .		2
261	EMI-immune analogue circuit generated through genetic evolution. Electronics Letters, 2009, 45, 199.	1.0	2
262	A memetic approach to the automatic design of high-performance analog integrated circuits. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-24.	2.6	32
263	Generic and Accurate Whitebox Behavioral Model for Fast Simulation of Analog Effects in Nanometer CMOS Digital Logic Circuits. IEEE Transactions on Electromagnetic Compatibility, 2009, 51, 351-357.	2.2	3
264	Optimised small-size tapered monopole antenna for pulsed ultra-wideband applications designed by a genetic algorithm. IET Microwaves, Antennas and Propagation, 2009, 3, 663.	1.4	8
265	A systematic design methodology for power-optimal design of high-order multi-bit continuous-time Delta-Sigma modulators. Analog Integrated Circuits and Signal Processing, 2009, 58, 215-225.	1.4	3
266	ANTIGONE: Top-down creation of analog-to-digital converter architectures. The Integration VLSI Journal, 2009, 42, 10-23.	2.1	4
267	Design of a 2Mbps FSK near-field transmitter for wireless capsule endoscopy. Sensors and Actuators A: Physical, 2009, 156, 43-48.	4.1	59
268	A reconfigurable, 0.13µm CMOS 110pJ/pulse, fully integrated IR-UWB receiver for communication and sub-cm ranging. , 2009, , .		23
269	A Fully Integrated Pinless Long-Range Power Supply with On-Chip Antenna for Scavenging-Based RFID Tag Powering. , 2009, , .		5
270	A methodology for measuring transistor ageing effects towards accurate reliability simulation. , 2009, , .		2

#	Article	IF	Citations
271	Ultra low power flash ADC for UWB transceiver applications. , 2009, , .		0
272	A 3-tier UWB-based indoor localization system for ultra-low-power sensor networks. IEEE Transactions on Wireless Communications, 2009, 8, 2813-2818.	9.2	30
273	Efficient size reduction technique for band-notched planar UWB monopole antennas. , 2009, , .		0
274	An Effective Technique for Symmetric Planar Monopole Antenna Miniaturization. IEEE Transactions on Antennas and Propagation, 2009, 57, 2989-2996.	5.1	38
275	A remote-powered RFID tag with 10Mb/s UWB uplink and −18.5dBm sensitivity UHF downlink in 0.18µm CMOS. , 2009, , .		49
276	A fuzzy selection based constraint handling method for multi-objective optimization of analog cells. , 2009, , .		7
277	Variation-Aware Analog Structural Synthesis. , 2009, , .		19
278	Mitigation of the sampling and substrate noise induced distortion in regenerative comparators by adaptive interpolation. , 2009, , .		0
279	Scalable Equivalent Circuit Modelling of the EM Field Coupling to Microstrips in the TEM Cell. , 2009, , .		4
280	Less expensive and high quality stopping criteria for MC-based analog IC yield optimization. , 2009, , .		1
281	RFID, Where are they?. , 2009, , .		3
282	A 0.4-1.4V 24MHz fully integrated 33µW, 104ppm/V supply-independent oscillator for RFIDs. , 2009, , .		12
283	Low-power sensor interfaces. , 2009, , .		0
284	Fuzzy selection based differential evolution algorithm for analog cell sizing capturing imprecise human intentions. , 2009, , .		1
285	RFID, where are they?. , 2009, , .		6
286	Template-Free Symbolic Performance Modeling of Analog Circuits via Canonical-Form Functions and Genetic Programming. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1162-1175.	2.7	49
287	Variation-Aware Structural Synthesis of Analog Circuits via Hierarchical Building Blocks and Structural Homotopy. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1281-1294.	2.7	41
288	Globally Reliable Variation-Aware Sizing of Analog Integrated Circuits via Response Surfaces and Structural Homotopy. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1627-1640.	2.7	41

#	Article	IF	Citations
289	A 70 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB Impulse Radio Receivers. IEEE Journal of Solid-State Circuits, 2009, 44, 1862-1871.	5.4	25
290	FEM-based investigation of spatial stimulation properties of a multi-electrode probe with micrometer-size electrodes for cortical and DBS applications. IFMBE Proceedings, 2009, , 154-157.	0.3	1
291	Automated Extraction of Expert Domain Knowledge from Genetic Programming Synthesis Results. Genetic and Evolutionary Computation, 2009, , 1-14.	1.0	0
292	A continuous-time delta-sigma modulator for 802.11a/b/g WLAN implemented with a hierarchical bottom-up optimization methodology. Analog Integrated Circuits and Signal Processing, 2008, 55, 37-45.	1.4	5
293	Analysis of quantization effects on high-order function neural networks. Applied Intelligence, 2008, 28, 51-67.	5.3	1
294	An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications. Microelectronics Reliability, 2008, 48, 1576-1580.	1.7	35
295	Classification of analog synthesis tools based on their architecture selection mechanisms. The Integration VLSI Journal, 2008, 41, 238-252.	2.1	42
296	Managing packet collisions in scavenging-based ULP transmit-only indoor localization systems. , 2008, , .		2
297	Miniaturization of UWB Antennas and its Influence on Antenna-Transceiver Performance. , 2008, , .		3
298	Impact of Antenna Type and Scaling on Scavenged Voltage in Passive RFID Tags. , 2008, , .		6
299	Importance sampled circuit learning ensembles for robust analog IC design. , 2008, , .		2
300	A 46pJ/pulse analog front-end in 130nm CMOS for UWB impulse radio receivers. , 2008, , .		4
301	Very fast methodology for the simulation of CMOS combinatorial circuits including noise. , 2008, , .		2
302	An efficient technique for UWB PTMA miniaturization. , 2008, , .		3
303	Automated extraction of expert knowledge in analog topology selection and sizing. , 2008, , .		7
304	A Design Approach for Power-Optimized Fully Reconfigurable $Delta Sigma$ A/D Converter for 4G Radios. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 229-233.	3.0	30
305	Impulse UWB antenna size reduction due to transmitter-antenna co-design. , 2008, , .		1
306	A modified small-size tapered monopole antenna for UWB applications designed by genetic algorithm. , 2008, , .		7

#	Article	IF	Citations
307	UWB antennas miniaturization and its influence on antenna-transceiver performance. , 2008, , .		0
308	A low-power mixing DAC IR-UWB-receiver. , 2008, , .		2
309	Simulation-based optimization of UGCs performances. , 2008, , .		13
310	Scaleable equivalent circuit modelling of the E-field coupling to microstrips in the TEM cell. , 2008, , .		5
311	Antenna Miniaturization Influence on the Performance of Impulse Radio UWB system. , 2008, , .		1
312	ISCLEs: Importance Sampled Circuit Learning Ensembles for Trustworthy Analog Circuit Topology Synthesis. Lecture Notes in Computer Science, 2008, , 11-21.	1.3	3
313	Genetic Programmingwith Reuse of Known Designs for Industrially Scalable, Novel Circuit Design. , 2008, , 159-184.		3
314	Assessment of the DPI Standard for Immunity Simulation of Integrated Circuits. , 2007, , .		9
315	System Design for Ultra-Low-Power UWB-based Indoor Localization. , 2007, , .		11
316	Methodology for fast identification of EMI-induced operating point shift in analogue circuits. Electronics Letters, 2007, 43, 1261.	1.0	1
317	Simultaneous multi-topology multi-objective sizing across thousands of analog circuit topologies. Proceedings - Design Automation Conference, 2007, , .	0.0	27
318	Scalable Gate-Level Models for Power and Timing Analysis. , 2007, , .		0
319	Future trends for wireless communication frontends in nanometer CMOS. , 2007, , .		0
320	Ultra-Low-Power Sensor Networks in Nanometer CMOS. , 2007, , .		11
321	A Simple Real-Coded Compact Genetic Algorithm and its Application to Antenna Optimization. , 2007, , .		11
322	Optimal Design Methodology for High-Order Continuous-Time Wideband Delta-Sigma Converters. , 2007, , .		1
323	Effect of Mismatch on Substrate Noise Coupling on Flash A/D Converters. , 2007, , .		0
324	A 3-Tier UWB-Based Indoor Localization Scheme for Ultra-Low-Power Sensor Nodes. , 2007, , .		6

#	Article	IF	Citations
325	Simultaneous Multi-Topology Multi-Objective Sizing Across Thousands of Analog Circuit Topologies. Proceedings - Design Automation Conference, 2007, , .	0.0	3
326	Guest Editorial [intro. to the special issue on the 2006 IEEE/ACM Design, Automation and Test in Europe Conference]. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 405-407.	2.7	0
327	A 14-bit 200-MHz Current-Steering DAC With Switching-Sequence Post-Adjustment Calibration. IEEE Journal of Solid-State Circuits, 2007, 42, 2386-2394.	5.4	89
328	Hierarchical Modeling, Optimization, and Synthesis for System-Level Analog and RF Designs. Proceedings of the IEEE, 2007, 95, 640-669.	21.3	198
329	The Analysis and Improvement of a Current-Steering DAC's Dynamic SFDR—II: The Output-Dependent Delay Differences. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 268-279.	0.1	58
330	Automated synthesis of complex analog circuits. , 2007, , .		10
331	Design tool solutions for mixed-signal/RF circuit design in CMOS nanometer technologies. , 2007, , .		11
332	Design strategy for Continous-Time Delta-Sigma based on power consideration for 4G radios. , 2007, , .		1
333	Analyzing the performance degradation of flash A/D converters due to substrate noise coupling. , 2007, , .		2
334	An Efficient Methodology for Hierarchical Synthesis of Mixed-Signal Systems with Fully Integrated Building Block Topology Selection. , 2007, , .		11
335	An Ultra-low-Power Quadrature PLL in 130nm CMOS for Impulse Radio Receivers. , 2007, , .		10
336	Resolving differences of parameter extraction methods for integrated inductor design and model validation. Analog Integrated Circuits and Signal Processing, 2007, 53, 71-79.	1.4	1
337	DESIGN OF AN ENERGY-EFFICIENT PULSED UWB RECEIVER. , 2007, , 303-329.		14
338	Tomorrow's analog: just dead or just different?. Proceedings - Design Automation Conference, 2006, , .	0.0	4
339	A Continuous-Time Delta-Sigma Modulator for 802.11a/b/g WLAN Implemented with a Hierarchical Bottom-up Optimization Methodology. , 2006, , .		2
340	Design methodologies and tools for circuit design in CMOS nanometer technologies. Solid-State Device Research Conference, 2008 ESSDERC 2008 38th European, 2006, , .	0.0	4
341	Efficient identification of major contributions to EMI-induced rectification effects in analog automotive circuits. , 2006, , .		11
342	Design methodologies and tools for circuit design in CMOS nanometer technologies. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2006, , .	0.0	1

#	Article	IF	Citations
343	Clock-skew-optimization methodology for substrate-noise reduction with supply-current folding. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 1146-1154.	2.7	12
344	Analyzing continuous-time /spl Delta//spl Sigma/ Modulators with generic behavioral models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 924-932.	2.7	17
345	The analysis and improvement of a current-steering DACs dynamic SFDR-I: the cell-dependent delay differences. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 3-15.	0.1	73
346	Evolution of substrate noise generation mechanisms with CMOS technology scaling. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 296-305.	0.1	37
347	Canonical form functions as a simple means for genetic programming to evolve human-interpretable functions. , 2006, , .		12
348	Hierarchical bottom--up analog optimization methodology validated by a delta--sigma A/D converter design for the 802.11a/b/g standard. , 2006, , .		10
349	Automation in mixed-signal design. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	3
350	Automation in Mixed-Signal Design: Challenges and Solutions in the Wake of the Nano Era. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	2
351	SWAN: high-level simulation methodology for digital substrate noise generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 23-33.	3.1	23
352	Genetic Programming in Industrial Analog CAD: Applications and Challenges. , 2006, , 291-306.		6
353	DESIGN METHODOLOGY AND MODEL GENERATION FOR COMPLEX ANALOG BLOCKS. , 2006, , 113-141.		1
354	Hierarchical bottom-up analog optimization methodology validated by a delta-sigma A/D converter design for the 802.11a/b/g standard. Proceedings - Design Automation Conference, 2006, , .	0.0	4
355	Phaseâ€“frequency transfer model of analogue and mixed-signal front-end architectures for system-level design. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 45.	1.6	2
356	CAD tools for embedded analogue circuits in mixed-signal integrated systems on chip. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 317.	1.6	52
357	Editorial: DATE04. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 1.	1.6	0
358	Digital ground bounce reduction by supply current shaping and clock frequency Modulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 65-76.	2.7	31
359	Performance space modeling for hierarchical synthesis of analog integrated circuits. , 2005, , .		36
360	An efficient, fully parasitic-aware power amplifier design optimization tool. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1526-1534.	0.1	25

#	Article	IF	Citations
361	Systematic top-down design of a low-power continuous-time delta-sigma modulator wideband CDMA. , 2005, , .		0
362	A reconfigurable delta sigma A/D convertor in 0.18Î¼m CMOS for flexible wireless receivers. , 2005, , .		1
363	Systematic analysis of the impact of nonidealities on a current-steering DACS SFDR. , 2005, , .		0
364	A CAD Platform for Sensor Interfaces in Low-Power Applications. Lecture Notes in Computer Science, 2005, , 374-381.	1.3	0
365	High-level simulation of substrate noise in high-ohmic substrates with interconnect and supply effects. , 2004, , .		13
366	Generalized Simulation-Based Posynomial Model Generation for Analog Integrated Circuits. Analog Integrated Circuits and Signal Processing, 2004, 40, 193-203.	1.4	13
367	Stability Analysis of Î”Î£ Modulators Using Wavelets. Analog Integrated Circuits and Signal Processing, 2004, 41, 279-291.	1.4	1
368	The PeopleMover educational project - design, simulation, and implementation of a real control system application. IEEE Control Systems, 2004, 24, 83-87.	0.8	4
369	Digital circuit capacitance and switching analysis for ground bounce in ICs with a high-ohmic substrate. IEEE Journal of Solid-State Circuits, 2004, 39, 1119-1130.	5.4	25
370	Systematic Design Exploration of Delta-Sigma ADCs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 86-95.	0.1	32
371	Efficient Analysis of Slow-Varying Oscillator Dynamics. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1457-1467.	0.1	8
372	A Gradient-Error and Edge-Effect Tolerant Switching Scheme for a High-Accuracy DAC. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 191-195.	0.1	46
373	An Analytical Integration Method for the Simulation of Continuous-Time<tex>$DeltaSigma$</tex>Modulators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 389-399.	2.7	26
374	Regression Criteria and Their Application in Different Modeling Cases. Analog Integrated Circuits and Signal Processing, 2003, 37, 113-122.	1.4	0
375	Fast Learning Algorithms for Feedforward Neural Networks. Applied Intelligence, 2003, 18, 37-54.	5.3	11
376	Peoplemover: an example of interdisciplinary project-based education in electrical engineering. IEEE Transactions on Education, 2003, 46, 157-167.	2.4	22
377	Design techniques and implementation of an 8-bit 200-MS/s interpolating/averaging CMOS A/D converter. IEEE Journal of Solid-State Circuits, 2003, 38, 483-494.	5.4	34
378	Modeling and experimental verification of substrate noise generation in a 220-kgates wlan system-on-chip with multiple supplies. IEEE Journal of Solid-State Circuits, 2003, 38, 1250-1260.	5.4	44

#	Article	IF	Citations
379	Watson: design space boundary exploration and model generation for analog and RF IC design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 213-224.	2.7	116
380	Simulation-based generation of posynomial performance models for the sizing of analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 517-534.	2.7	131
381	Behavioral modeling of (coupled) harmonic oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 1017-1026.	2.7	22
382	A high-level simulation and synthesis environment for Î”Î£ modulators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 1049-1061.	2.7	82
383	THE EFFECTS OF QUANTIZATION ON MULTI-LAYER FEEDFORWARD NEURAL NETWORKS. International Journal of Pattern Recognition and Artificial Intelligence, 2003, 17, 637-661.	1.2	7
384	Architectural selection of A/D converters. , 2003, , .		17
385	Efficient DDD-based symbolic analysis of linear analog circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 474-487.	2.2	19
386	Behavioral modeling of (coupled) harmonic oscillators. Proceedings - Design Automation Conference, 2002, , .	0.0	8
387	Techniques and Applications of Symbolic Analysis for Analog Integrated Circuits. , 2002, , 953-984.		6
388	Circuit simplification for the symbolic analysis of analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 395-407.	2.7	51
389	Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification. IEEE Journal of Solid-State Circuits, 2002, 37, 1065-1072.	5.4	81
390	Methodology and experimental verification for substrate noise reduction in CMOS mixed-signal ICs with synchronous digital circuits. IEEE Journal of Solid-State Circuits, 2002, 37, 1383-1395.	5.4	62
391	Modeling and analysis techniques for system-level architectural design of telecom front-ends. IEEE Transactions on Microwave Theory and Techniques, 2002, 50, 360-368.	4.6	49
392	Power estimation methods for analog circuits for architectural exploration of integrated systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 155-162.	3.1	47
393	A layout synthesis methodology for array-type analog blocks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 645-661.	2.7	11
394	Symbolic modeling of periodically time-varying systems using harmonic transfer matrices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 1011-1024.	2.7	54
395	CYCLONE: automated design and layout of RF LC-oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 1161-1170.	2.7	63
396	Systematic Design of High-Performance Data Converters. , 2002, , 591-612.		0

#	Article	IF	Citations
397	Braille to print translations for Chinese. Information and Software Technology, 2002, 44, 91-100.	4.4	17
398	A fast learning algorithm for time-delay neural networks. Information Sciences, 2002, 148, 27-39.	6.9	16
399	Title is missing!. Analog Integrated Circuits and Signal Processing, 2002, 31, 119-130.	1.4	4
400	Computer-Aided Design of Analog Integrated Circuits and Systems. , 2002, , .		38
401	Analog Power Modeling for Data Converters and Filters. , 2002, , 613-629.		0
402	AMGIE-A synthesis environment for CMOS analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 1037-1058.	2.7	106
403	A CMOS multiparameter biochemical microsensor with temperature control and signal interfacing. IEEE Journal of Solid-State Circuits, 2001, 36, 2030-2038.	5.4	70
404	Models and Analysis Techniques for Systematic Design and Verification of Frequency Synthesizers. , 2001, , 107-129.		0
405	Nonlinear Symbolic Network Analysis: Algorithms and Applications to RF Circuits. , 2001, , 131-154.		0
406	Efficient DDD-based symbolic analysis of large linear analog circuits. , 2001, , .		19
407	Analog small-signal modeling-part I: behavioral signal path modeling for analog integrated circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 701-711.	2.2	18
408	Systematic design of high-accuracy current-steering D/A converter macrocells for integrated VLSI systems. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 300-309.	2.2	26
409	Analog small-signal modeling-part II: elementary transistor stages analyzed with behavioral signal path modeling. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 712-721.	2.2	10
410	Efficient High-Level Simulation of Analog Telecom Frontends. , 2001, , 61-81.		0
411	Modeling and realisation of high accuracy, high speed current-steering CMOS D/A converters. Measurement: Journal of the International Measurement Confederation, 2000, 28, 123-138.	5.0	3
412	Computer-aided design of analog and mixed-signal integrated circuits. Proceedings of the IEEE, 2000, 88, 1825-1854.	21.3	461
413	Optimal RF design using smart evolutionary algorithms. , 2000, , .		28
414	CYCLONE. , 2000, , .		17

#	Article	IF	Citations
415	Systematic design of a 14-bit 150-MS/s CMOS current-steering D/A converter. , 2000, , .		6
416	Models for systematic design and verification of frequency synthesizers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1301-1308.	2.2	12
417	Behavioral model of reusable D/A converters. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1323-1326.	2.2	16
418	High-frequency distortion analysis of analog integrated circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 335-345.	2.2	109
419	Evaluation of error-control strategies for the linear symbolic analysis of analog integrated circuits. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 594-606.	0.1	17
420	A 14-bit intrinsic accuracy Q/sup 2/ random walk CMOS DAC. IEEE Journal of Solid-State Circuits, 1999, 34, 1708-1718.	5.4	252
421	Top-Down Design of Mixed-Mode Systems: Challenges and Solutions. , 1999, , 269-300.		12
422	Analog Layout Generation for Performance and Manufacturability. , 1999, , .		79
423	Probabilistic fault detection and the selection of measurements for analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 862-872.	2.7	29
424	Symbolic network analysis methods for practical analog integrated circuits: a survey. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1331-1341.	2.2	36
425	Symbolic analysis of large analog circuits using a sensitivity-driven enumeration of common spanning trees. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1342-1350.	2.2	15
426	A fully integrated low-power CMOS particle detector front-end for space applications. IEEE Transactions on Nuclear Science, 1998, 45, 2272-2278.	2.0	26
427	Guest Editorial Special Section On Symbolic Circuit Analysis Techniques. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1330-1330.	2.2	0
428	High-Level Power Minimization of Analog Sensor Interface Architectures. Integrated Computer-Aided Engineering, 1998, 5, 303-314.	4.6	2
429	Symbolic Analysis Techniques. , 1998, , .		72
430	CAD tools for data converter design: an overview. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1996, 43, 77-89.	2.2	36
431	Optimal fault detection for analogue circuits under manufacturing tolerances. Electronics Letters, 1996, 32, 33.	1.0	2
432	Using top-down CAD tools for mixed analog/digital ASICs: a practical design case. Analog Integrated Circuits and Signal Processing, 1996, 10, 101-117.	1.4	20

#	Article	IF	Citations
433	Synthesis tools for mixed-signal ICs. , 1996, , .		48
434	An analogue module generator for mixed analogue/digital asic design. International Journal of Circuit Theory and Applications, 1995, 23, 269-283.	2.0	43
435	Efficient symbolic computation of approximated small-signal characteristics of analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 327-330.	5.4	71
436	A performance-driven placement tool for analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 773-780.	5.4	120
437	Algorithm for efficient symbolic analysis of large analogue circuits. Electronics Letters, 1994, 30, 1108-1109.	1.0	11
438	Symbolic analysis methods and applications for analog circuits: a tutorial overview. Proceedings of the IEEE, 1994, 82, 287-304.	21.3	161
439	Symbolic Analysis for Automated Design of Analog Integrated Circuits. , 1991, , .		239
440	Analog circuit design optimization based on symbolic simulation and simulated annealing. IEEE Journal of Solid-State Circuits, 1990, 25, 707-713.	5.4	212
441	ISAAC: a symbolic simulator for analog integrated circuits. IEEE Journal of Solid-State Circuits, 1989, 24, 1587-1597.	5.4	234
442	A phase-frequency transfer description of analog and mixed-signal front-end architectures for system-level design. , 0, , .		0
443	An opamp as a tool for testing. , 0, , .		1
444	An intelligent analog IC design system based on manipulation of design equations. , 0, , .		25
445	An intelligent design system for analogue integrated circuit. , 0, , .		14
446	A behavioral representation for Nyquist rate A/D converters. , 0, , .		22
447	Interactive symbolic distortion analysis of analogue integrated circuits. , 0, , .		2
448	Symbolic approximation strategies and the symbolic analysis of large and nonlinear circuits. , 0, , .		12
449	A design tool for weakly nonlinear analog integrated circuits with multiple inputs (mixers,) Tj ETQq1 1 0.784314 rgBT /Overlock 10 Tf		10
450	Analog behavioral models for simulation and synthesis of mixed-signal systems. , 0, , .		6

#	Article	IF	Citations
451	Modeling of the power-supply interactions of CMOS operational amplifiers using symbolic computation. , 0, , .		1
452	Pleasures, perils and pitfalls of symbolic analysis. , 0, , .		1
453	Symbolic analysis of large analog integrated circuits by approximation during expression generation. , 0, , .		21
454	A methodology for analog design automation in mixed-signal ASICs. , 0, , .		14
455	A methodology for analog high-level synthesis. , 0, , .		4
456	Efficient symbolic computation of approximated small-signal characteristics. , 0, , .		11
457	Testing of analog integrated circuits based on power-supply current monitoring and discrimination analysis. , 0, , .		15
458	A flexible topology selection program as part of an analog synthesis system. , 0, , .		18
459	Direct performance-driven placement of mismatch-sensitive analog circuits. , 0, , .		1
460	Analog routing for manufacturability. , 0, , .		16
461	Synthesis tools for Mixed-Signal ICs: progress on frontend and backend strategies. , 0, , .		29
462	EsteMate: a tool for automated power and area estimation in analog top-down design and synthesis. , 0, , .		13
463	Thermally constrained placement of smart-power IC's and multi-chip modules. , 0, , .		7
464	Automated test pattern generation for analog integrated circuits. , 0, , .		20
465	High-level synthesis of analog sensor interface front-ends. , 0, , .		1
466	Efficient yield estimation within automated analog IC design. , 0, , .		3
467	A 12 bit 200 MHz low glitch CMOS D/A converter. , 0, , .		23
468	Efficient symbolic analysis of large analog circuits using sensitivity-driven ranking of matroid intersections. , 0, , .		1

#	Article	IF	Citations
469	Modeling and simulation for low power in mixed-signal integrated systems. , 0, , .		2
470	Mondriaan: a tool for automated layout synthesis of array-type analog blocks. , 0, , .		15
471	Efficient symbolic analysis of analog integrated circuits using determinant decision diagrams. , 0, , .		2
472	System-level design tools for RF communication ICs. , 0, , .		3
473	Nonlinear behavioral modeling and phase noise evaluation in phase locked loops. , 0, , .		15
474	Behavioral model for D/A converters as VSI virtual components. , 0, , .		3
475	Efficient statistical analog IC design using symbolic methods. , 0, , .		5
476	Transforming small-signal modeling into control system modeling. , 0, , .		1
477	A power estimation model for high-speed CMOS A/D converters. , 0, , .		7
478	A 14 b 150 Msample/s update rate Q/sup 2/ random walk CMOS DAC. , 0, , .		4
479	Statistical behavioral modeling for A/D-converters. , 0, , .		12
480	BANDIT: embedding analog-to-digital converters on digital telecom ASICs. , 0, , .		0
481	System-level analysis of RF transceiver-integrated circuits. , 0, , .		2
482	Circuit complexity reduction for symbolic analysis of analog integrated circuits. , 0, , .		6
483	High-level simulation and power modelling of mixed-signal front-ends for digital telecommunications. , 0, , .		9
484	Efficient analysis of the stability of sigma-delta modulators using wavelets. , 0, , .		3
485	Modeling and simulation of a sigma-delta digital to analog converter using VHDL-AMS. , 0, , .		11
486	Evaluation of the substrate noise effect on analog circuits in mixed-signal designs. , 0, , .		8

#	Article	IF	Citations
487	ACTIF: a high-level power estimation tool for Analog Continuous-Time Filters. , 0, , .		6
488	DAISY: a simulation-based high-level synthesis tool for Î”Î£ modulators. , 0, , .		21
489	High-level design case of a switched-capacitor low-pass filter using Verilog-A. , 0, , .		2
490	Systematic design of data converters. , 0, , .		2
491	Simulation-based automatic generation of signomial and posynomial performance models for analog integrated circuit sizing. , 0, , .		23
492	A layout-aware synthesis methodology for RF circuits. , 0, , .		53
493	High-level simulation of substrate noise generation from large digital circuits with multiple supplies. , 0, , .		7
494	Dedicated system-level simulation of Î”Î£ modulators. , 0, , .		3
495	Efficient time-domain simulation of telecom frontends using a complex damped exponential signal model. , 0, , .		3
496	The effects of quantization on high order function neural networks. , 0, , .		0
497	CAD solutions and outstanding challenges for mixed-signal and RF IC design. , 0, , .		37
498	Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification. , 0, , .		3
499	A CMOS multi-parameter biochemical microsensor with temperature control and signal interfacing. , 0, , .		0
500	Analyzing the impact of substrate noise on embedded analog-to-digital converters. , 0, , .		14
501	Constructing symbolic models for the input/output behavior of periodically time-varying systems using harmonic transfer matrices. , 0, , .		8
502	Power optimization in Î£Î” ADC design. , 0, , .		1
503	Methodology and experimental verification for substrate noise reduction in CMOS mixed-signal ICs with synchronous digital circuits. , 0, , .		1
504	Fast, exploration of Î”Î£ADC design space. , 0, , .		0

#	Article	IF	Citations
505	DAISY-CT: a high-level simulation tool for continuous-time Î”Î£ modulators. , 0, , .		2
506	Efficient time-domain simulation of continuous-time Î”Î£ A/D converters using analytical integration. , 0, , .		2
507	A behavioral simulation tool for continuous-time Î”Î£ modulators. , 0, , .		7
508	Regression criteria and their application in different modeling cases. , 0, , .		2
509	On the difference between two widely publicized methods for analyzing oscillator phase behavior. , 0, , .		26
510	OFDM-WLAN receiver performance improvement using digital compensation techniques. , 0, , .		11
511	A fitting approach to generate symbolic expressions for linear and nonlinear analog circuit performance characteristics. , 0, , .		12
512	WATSON: a multi-objective design space exploration tool for analog and RF IC design. , 0, , .		3
513	A 8-bit 200 MS/s interpolating/averaging CMOS A/D converter. , 0, , .		10
514	Systematic design of a 200 MS/s 8-bit interpolating A/D converter. , 0, , .		2
515	RoCFaST: a method of speeding up simulation of Î”Î£ modulators using state-space tracking. , 0, , .		0
516	Modelling impact of digital substrate noise on embedded regenerative comparators. , 0, , .		11
517	Digital circuit capacitance and switching analysis for ground bounce in ICs with a high-ohmic substrate. , 0, , .		8
518	Modelling of the impact of the current source output impedance on the SFDR of current-steering CMOS D/A converters. , 0, , .		1
519	Fast, layout-inclusive analog circuit synthesis using pre-compiled parasitic-aware symbolic performance models. , 0, , .		33
520	Performance modeling of analog integrated circuits using least-squares support vector machines. , 0, , .		43
521	Digital ground bounce reduction by phase modulation of the clock. , 0, , .		6
522	High-level modeling of continuous-time Î”Î£ A/D-converters using formal models. , 0, , .		1

#	Article	IF	Citations
523	Impact of technology scaling on substrate noise generation mechanisms [mixed signal ICs]. , 0, , .		5
524	Knowledge- and optimization-based design of RF power amplifiers. , 0, , .		1
525	A 14-bit 130-MHz CMOS current-steering DAC with adjustable INL. , 0, , .		15
526	CAFFEINE: Template-Free Symbolic Model Generation of Analog Circuits via Canonical Form Functions and Genetic Programming. , 0, , .		33
527	IBMG: Interpretable Behavioral Model Generator for Nonlinear Analog Circuits via Canonical Form Functions and Genetic Programming. , 0, , .		4
528	Behavioral modeling and simulation of weakly nonlinear sampled-data systems. , 0, , .		2
529	Efficient Multiobjective Synthesis of Analog Circuits using Hierarchical Pareto-Optimal Performance Hypersurfaces. , 0, , .		76
530	CAFFEINE: template-free symbolic model generation of analog circuits via canonical form functions and genetic programming. , 0, , .		5
531	Time-Domain Simulation of Sampled Weakly Nonlinear Systems Using Analytical Integration and Orthogonal Polynomial Series. , 0, , .		1
532	Analog and Digital Circuit Design in 65 nm CMOS: End of the Road?. , 0, , .		39
533	Analysis of Simulation-Driven Numerical Performance Modeling Techniques for Application to Analog Circuit Optimization. , 0, , .		34
534	Assessment of parameter extraction methods for integrated inductor design and model validation. , 0, , .		2
535	A Behavioral Model of Sampled-Data Systems in the Phase-Frequency Transfer Domain for Architectural Exploration of Transceivers. , 0, , .		1
536	A novel method for the fault detection of analog integrated circuits. , 0, , .		14
537	An efficient DC root solving algorithm with guaranteed convergence for analog integrated CMOS circuits. , 0, , .		1
538	Efficient analog circuit synthesis with simultaneous yield and robustness optimization. , 0, , .		3