

# Georges G E Gielen

## List of Publications by Year in descending order

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538  
papers

10,340  
citations

53794

45  
h-index

74163

75  
g-index

572  
all docs

572  
docs citations

572  
times ranked

4900  
citing authors

#	ARTICLE	IF	CITATIONS
1	Computer-aided design of analog and mixed-signal integrated circuits. Proceedings of the IEEE, 2000, 88, 1825-1854.	21.3	461
2	A Gaussian Process Surrogate Model Assisted Evolutionary Algorithm for Medium Scale Expensive Optimization Problems. IEEE Transactions on Evolutionary Computation, 2014, 18, 180-192.	10.0	379
3	A 14-bit intrinsic accuracy $Q/\text{sup } 2/$ random walk CMOS DAC. IEEE Journal of Solid-State Circuits, 1999, 34, 1708-1718.	5.4	252
4	Symbolic Analysis for Automated Design of Analog Integrated Circuits. , 1991, , .		239
5	ISAAC: a symbolic simulator for analog integrated circuits. IEEE Journal of Solid-State Circuits, 1989, 24, 1587-1597.	5.4	234
6	Analog circuit design optimization based on symbolic simulation and simulated annealing. IEEE Journal of Solid-State Circuits, 1990, 25, 707-713.	5.4	212
7	An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe. IEEE Journal of Solid-State Circuits, 2014, 49, 248-261.	5.4	208
8	Hierarchical Modeling, Optimization, and Synthesis for System-Level Analog and RF Designs. Proceedings of the IEEE, 2007, 95, 640-669.	21.3	198
9	An Efficient Method for Antenna Design Optimization Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Antennas and Propagation, 2014, 62, 7-18.	5.1	194
10	Symbolic analysis methods and applications for analog circuits: a tutorial overview. Proceedings of the IEEE, 1994, 82, 287-304.	21.3	161
11	A Review on Internet of Things Solutions for Intelligent Energy Control in Buildings for Smart City Applications. Energy Procedia, 2017, 111, 770-779.	1.8	147
12	Simulation-based generation of posynomial performance models for the sizing of analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 517-534.	2.7	131
13	A performance-driven placement tool for analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 773-780.	5.4	120
14	Watson: design space boundary exploration and model generation for analog and RF IC design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 213-224.	2.7	116
15	High-frequency distortion analysis of analog integrated circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 335-345.	2.2	109
16	AMGIE-A synthesis environment for CMOS analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 1037-1058.	2.7	106
17	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	5.4	101
18	Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 793-805.	2.7	93

#	ARTICLE	IF	CITATIONS
19	A 14-bit 200-MHz Current-Steering DAC With Switching-Sequence Post-Adjustment Calibration. IEEE Journal of Solid-State Circuits, 2007, 42, 2386-2394.	5.4	89
20	A high-level simulation and synthesis environment for $\Gamma$ - $\Sigma$ modulators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 1049-1061.	2.7	82
21	Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification. IEEE Journal of Solid-State Circuits, 2002, 37, 1065-1072.	5.4	81
22	High-performance a-In-Ga-Zn-O Schottky diode with oxygen-treated metal contacts. Applied Physics Letters, 2012, 101, .	3.3	81
23	GASPAD: A General and Efficient mm-Wave Integrated Circuit Synthesis Method Based on Surrogate Model Assisted Evolutionary Algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 169-182.	2.7	79
24	Analog Layout Generation for Performance and Manufacturability. , 1999, , .		79
25	Efficient Multiobjective Synthesis of Analog Circuits using Hierarchical Pareto-Optimal Performance Hypersurfaces. , 0, , .		76
26	The analysis and improvement of a current-steering DACs dynamic SFDR-I: the cell-dependent delay differences. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 3-15.	0.1	73
27	Symbolic Analysis Techniques. , 1998, , .		72
28	Efficient symbolic computation of approximated small-signal characteristics of analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 327-330.	5.4	71
29	A CMOS multiparameter biochemical microsensor with temperature control and signal interfacing. IEEE Journal of Solid-State Circuits, 2001, 36, 2030-2038.	5.4	70
30	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	14.6	70
31	Far-Field On-Chip Antennas Monolithically Integrated in a Wireless-Powered 5.8-GHz Downlink/UWB Uplink RFID Tag in 0.18- $\mu\text{m}$ Standard CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1746-1758.	5.4	67
32	A Multichannel Integrated Circuit for Electrical Recording of Neural Activity, With Independent Channel Programmability. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 101-110.	4.0	66
33	Computer-Aided Analog Circuit Design for Reliability in Nanometer CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 50-58.	3.6	65
34	Gigahertz Operation of a-IGZO Schottky Diodes. IEEE Transactions on Electron Devices, 2013, 60, 3407-3412.	3.0	64
35	CYCLONE: automated design and layout of RF LC-oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 1161-1170.	2.7	63
36	Synthesis of Integrated Passive Components for High-Frequency RF ICs Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1458-1468.	2.7	63

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37	Methodology and experimental verification for substrate noise reduction in CMOS mixed-signal ICs with synchronous digital circuits. IEEE Journal of Solid-State Circuits, 2002, 37, 1383-1395.	5.4	62
38	A 42 fJ/Step-FoM Two-Step VCO-Based Delta-Sigma ADC in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 714-723.	5.4	61
39	Design of a 2Mbps FSK near-field transmitter for wireless capsule endoscopy. Sensors and Actuators A: Physical, 2009, 156, 43-48.	4.1	59
40	Effect of temperature on phosphorus sorption to sediments from shallow eutrophic lakes. Ecological Engineering, 2011, 37, 1515-1522.	3.6	59
41	The Analysis and Improvement of a Current-Steering DAC's Dynamic SFDR—II: The Output-Dependent Delay Differences. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 268-279.	0.1	58
42	Symbolic modeling of periodically time-varying systems using harmonic transfer matrices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 1011-1024.	2.7	54
43	A layout-aware synthesis methodology for RF circuits. , 0, , .		53
44	An Efficient High-Frequency Linear RF Amplifier Synthesis Method Based on Evolutionary Computation and Machine Learning Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 981-993.	2.7	53
45	CAD tools for embedded analogue circuits in mixed-signal integrated systems on chip. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 317.	1.6	52
46	Supply-Noise-Resilient Design of a BBPLL-Based Force-Balanced Wheatstone Bridge Interface in 130-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2618-2627.	5.4	52
47	Circuit simplification for the symbolic analysis of analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 395-407.	2.7	51
48	Modeling and analysis techniques for system-level architectural design of telecom front-ends. IEEE Transactions on Microwave Theory and Techniques, 2002, 50, 360-368.	4.6	49
49	A remote-powered RFID tag with 10Mb/s UWB uplink and $\approx 18.5$ dBm sensitivity UHF downlink in 0.18 $\mu$ m CMOS. , 2009, , .		49
50	Template-Free Symbolic Performance Modeling of Analog Circuits via Canonical-Form Functions and Genetic Programming. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1162-1175.	2.7	49
51	Synthesis tools for mixed-signal ICs. , 1996, , .		48
52	A Reconfigurable, 130 nm CMOS 108 pJ/pulse, Fully Integrated IR-UWB Receiver for Communication and Precise Ranging. IEEE Journal of Solid-State Circuits, 2010, 45, 69-83.	5.4	48
53	Power estimation methods for analog circuits for architectural exploration of integrated systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 155-162.	3.1	47
54	A Gradient-Error and Edge-Effect Tolerant Switching Scheme for a High-Accuracy DAC. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 191-195.	0.1	46

#	ARTICLE	IF	CITATIONS
55	A fully-digital, 0.3V, 270 nW capacitive sensor interface without external references. , 2011, , .		46
56	Trustworthy Genetic Programming-Based Synthesis of Analog Circuit Topologies Using Hierarchical Domain-Specific Building Blocks. IEEE Transactions on Evolutionary Computation, 2011, 15, 557-570.	10.0	45
57	Modeling and experimental verification of substrate noise generation in a 220-k gates wlan system-on-chip with multiple supplies. IEEE Journal of Solid-State Circuits, 2003, 38, 1250-1260.	5.4	44
58	An Integrated a-IGZO UHF Energy Harvester for Passive RFID Tags. IEEE Transactions on Electron Devices, 2014, 61, 3289-3295.	3.0	44
59	A 0.6-V, 0.015-mm <sup>2</sup> , Time-Based ECG Readout for Ambulatory Applications in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 298-308.	5.4	44
60	An analogue module generator for mixed analogue/digital asic design. International Journal of Circuit Theory and Applications, 1995, 23, 269-283.	2.0	43
61	Performance modeling of analog integrated circuits using least-squares support vector machines. , 0, , .		43
62	An Efficient Evolutionary Algorithm for Chance-Constrained Bi-Objective Stochastic Optimization. IEEE Transactions on Evolutionary Computation, 2013, 17, 786-796.	10.0	43
63	Closed-loop optical neural stimulation based on a 32-channel low-noise recording system with online spike sorting. Journal of Neural Engineering, 2014, 11, 046005.	3.5	43
64	Classification of analog synthesis tools based on their architecture selection mechanisms. The Integration VLSI Journal, 2008, 41, 238-252.	2.1	42
65	Efficient Reciprocity-Based Algorithm to Predict Worst Case Induced Disturbances on Multiconductor Transmission Lines due to Incoming Plane Waves. IEEE Transactions on Electromagnetic Compatibility, 2013, 55, 208-216.	2.2	42
66	Variation-Aware Structural Synthesis of Analog Circuits via Hierarchical Building Blocks and Structural Homotopy. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1281-1294.	2.7	41
67	Globally Reliable Variation-Aware Sizing of Analog Integrated Circuits via Response Surfaces and Structural Homotopy. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1627-1640.	2.7	41
68	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS-Part 1: Basic Principles. IEEE Solid-State Circuits Magazine, 2020, 12, 47-55.	0.4	41
69	Analog and Digital Circuit Design in 65 nm CMOS: End of the Road?. , 0, , .		39
70	High-Performance a-IGZO Thin Film Diode as Selector for Cross-Point Memory Application. IEEE Electron Device Letters, 2014, 35, 642-644.	3.9	39
71	An Effective Technique for Symmetric Planar Monopole Antenna Miniaturization. IEEE Transactions on Antennas and Propagation, 2009, 57, 2989-2996.	5.1	38
72	Computer-Aided Design of Analog Integrated Circuits and Systems. , 2002, , .		38

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73	CAD solutions and outstanding challenges for mixed-signal and RF IC design. , 0, , .		37
74	Evolution of substrate noise generation mechanisms with CMOS technology scaling. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 296-305.	0.1	37
75	Transistor aging-induced degradation of analog circuits: Impact analysis and design guidelines. , 2011, , .		37
76	CAD tools for data converter design: an overview. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1996, 43, 77-89.	2.2	36
77	Symbolic network analysis methods for practical analog integrated circuits: a survey. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1331-1341.	2.2	36
78	Performance space modeling for hierarchical synthesis of analog integrated circuits. , 2005, , .		36
79	Efficient Variability-Aware NBTI and Hot Carrier Circuit Reliability Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1884-1893.	2.7	36
80	An integrated multi-electrode-optrode array for in vitro optogenetics. Scientific Reports, 2016, 6, 20353.	3.3	36
81	An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications. Microelectronics Reliability, 2008, 48, 1576-1580.	1.7	35
82	Design techniques and implementation of an 8-bit 200-MS/s interpolating/averaging CMOS A/D converter. IEEE Journal of Solid-State Circuits, 2003, 38, 483-494.	5.4	34
83	Analysis of Simulation-Driven Numerical Performance Modeling Techniques for Application to Analog Circuit Optimization. , 0, , .		34
84	Fast, layout-inclusive analog circuit synthesis using pre-compiled parasitic-aware symbolic performance models. , 0, , .		33
85	CAFFEINE: Template-Free Symbolic Model Generation of Analog Circuits via Canonical Form Functions and Genetic Programming. , 0, , .		33
86	Systematic Design Exploration of Delta-Sigma ADCs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 86-95.	0.1	32
87	A memetic approach to the automatic design of high-performance analog integrated circuits. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-24.	2.6	32
88	Digital ground bounce reduction by supply current shaping and clock frequency Modulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 65-76.	2.7	31
89	Automated Design of Analog and High-frequency Circuits. Studies in Computational Intelligence, 2014, , .	0.9	31
90	A Design Approach for Power-Optimized Fully Reconfigurable $\Delta\Sigma$ A/D Converter for 4G Radios. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 229-233.	3.0	30

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91	A 3-tier UWB-based indoor localization system for ultra-low-power sensor networks. IEEE Transactions on Wireless Communications, 2009, 8, 2813-2818.	9.2	30
92	Calibration of DAC Mismatch Errors in $\Sigma\Delta$ ADCs Based on a Sine-Wave Measurement. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 567-571.	3.0	30
93	An implantable 455-active-electrode 52-channel CMOS neural probe. , 2013, , .		30
94	Synthesis tools for Mixed-Signal ICs: progress on frontend and backend strategies. , 0, , .		29
95	Probabilistic fault detection and the selection of measurements for analog integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 862-872.	2.7	29
96	A cryogenic analog to digital converter operating from 300 K down to 4.4 K. Review of Scientific Instruments, 2010, 81, 024702.	1.3	29
97	An enhanced MOEA/D-DE and its application to multiobjective analog cell sizing. , 2010, , .		29
98	Low Loss CMOS-Compatible PECVD Silicon Nitride Waveguides and Grating Couplers for Blue Light Optogenetic Applications. IEEE Photonics Journal, 2016, 8, 1-11.	2.0	29
99	Optimal RF design using smart evolutionary algorithms. , 2000, , .		28
100	Analog circuit reliability in sub-32 nanometer CMOS: Analysis and mitigation. , 2011, , .		28
101	Simultaneous multi-topology multi-objective sizing across thousands of analog circuit topologies. Proceedings - Design Automation Conference, 2007, , .	0.0	27
102	A fully integrated low-power CMOS particle detector front-end for space applications. IEEE Transactions on Nuclear Science, 1998, 45, 2272-2278.	2.0	26
103	Systematic design of high-accuracy current-steering D/A converter macrocells for integrated VLSI systems. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 300-309.	2.2	26
104	On the difference between two widely publicized methods for analyzing oscillator phase behavior. , 0, , .		26
105	An Analytical Integration Method for the Simulation of Continuous-Time $\Sigma\Delta$ Modulators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 389-399.	2.7	26
106	An intelligent analog IC design system based on manipulation of design equations. , 0, , .		25
107	Digital circuit capacitance and switching analysis for ground bounce in ICs with a high-ohmic substrate. IEEE Journal of Solid-State Circuits, 2004, 39, 1119-1130.	5.4	25
108	An efficient, fully parasitic-aware power amplifier design optimization tool. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1526-1534.	0.1	25

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109	A 70 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB Impulse Radio Receivers. IEEE Journal of Solid-State Circuits, 2009, 44, 1862-1871.	5.4	25
110	Deep-level transient spectroscopy on an amorphous InGaZnO <sub>4</sub> Schottky diode. Applied Physics Letters, 2014, 104, 082112.	3.3	24
111	A 12 bit 200 MHz low glitch CMOS D/A converter. , 0, , .		23
112	Simulation-based automatic generation of signomial and posynomial performance models for analog integrated circuit sizing. , 0, , .		23
113	SWAN: high-level simulation methodology for digital substrate noise generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 23-33.	3.1	23
114	A reconfigurable, 0.13m CMOS 110pJ/pulse, fully integrated IR-UWB receiver for communication and sub-cm ranging. , 2009, , .		23
115	Stochastic Macromodeling of Nonlinear Systems Via Polynomial Chaos Expansion and Transfer Function Trajectories. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 1454-1460.	4.6	23
116	Magnetic hysteresis at the domain scale of a multi-scale material model for magneto-elastic behaviour. Journal of Magnetism and Magnetic Materials, 2016, 414, 168-179.	2.3	23
117	A behavioral representation for Nyquist rate A/D converters. , 0, , .		22
118	Peplemover: an example of interdisciplinary project-based education in electrical engineering. IEEE Transactions on Education, 2003, 46, 157-167.	2.4	22
119	Behavioral modeling of (coupled) harmonic oscillators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 1017-1026.	2.7	22
120	A 2.8-to-8.5mW GSM/bluetooth/UMTS/DVB-H/WLAN fully reconfigurable CT&#x0394;&#x03A3; with 200kHz to 20MHz BW for 4G radios in 90nm digital CMOS. , 2010, , .		22
121	A novel, PLL-based frequency-to-digital conversion mechanism for sensor interfaces. Sensors and Actuators A: Physical, 2011, 172, 220-227.	4.1	22
122	A 40-MHz Bandwidth 0â€²2 MASH VCO-Based Delta-Sigma ADC With 35-fJ/Step FoM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 952-956.	3.0	22
123	Symbolic analysis of large analog integrated circuits by approximation during expression generation. , 0, , .		21
124	DAISY: a simulation-based high-level synthesis tool for Î”Î” modulators. , 0, , .		21
125	Efficient reliability simulation of analog ICs including variability and time-varying stress. , 2009, , .		21
126	UHF IGZO Schottky diode. , 2012, , .		21



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127	Integral equations formulation of plasmonic transmission lines. Optics Express, 2014, 22, 22388.	3.4	21
128	Using top-down CAD tools for mixed analog/digital ASICs: a practical design case. Analog Integrated Circuits and Signal Processing, 1996, 10, 101-117.	1.4	20
129	Automated test pattern generation for analog integrated circuits. , 0, , .		20
130	Far-field RF powering system for RFID and implantable devices with monolithically integrated on-chip antenna. , 2010, , .		20
131	Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 577-586.	5.4	20
132	A Low-Complexity Radar Detector Outperforming OS-CFAR for Indoor Drone Obstacle Avoidance. IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing, 2021, 14, 9162-9175.	4.9	20
133	Efficient DDD-based symbolic analysis of large linear analog circuits. , 2001, , .		19
134	Efficient DDD-based symbolic analysis of linear analog circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 474-487.	2.2	19
135	Massively multi-topology sizing of analog integrated circuits. , 2009, , .		19
136	Variation-Aware Analog Structural Synthesis. , 2009, , .		19
137	Design and test of analog circuits towards sub-ppm level. , 2014, , .		19
138	Effective DC fault models and testing approach for open defects in analog circuits. , 2016, , .		19
139	A flexible topology selection program as part of an analog synthesis system. , 0, , .		18
140	Analog small-signal modeling-part I: behavioral signal path modeling for analog integrated circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 701-711.	2.2	18
141	Experimental demonstration of a fully digital capacitive sensor interface built entirely using carbon-nanotube FETs. , 2013, , .		18
142	Performance Analysis of Energy-Efficient BBPLL-Based Sensor-to-Digital Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2130-2138.	5.4	18
143	Behavioral study of the surrogate model-aware evolutionary search framework. , 2014, , .		18
144	Understanding the Impact of Time-Dependent Random Variability on Analog ICs: From Single Transistor Measurements to Circuit Simulations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 601-610.	3.1	18

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145	Evaluation of error-control strategies for the linear symbolic analysis of analog integrated circuits. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 594-606.	0.1	17
146	CYCLONE. , 2000, , .		17
147	Braille to print translations for Chinese. Information and Software Technology, 2002, 44, 91-100.	4.4	17
148	Architectural selection of A/D converters. , 2003, , .		17
149	Analyzing continuous-time $\Delta\Sigma$ Modulators with generic behavioral models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 924-932.	2.7	17
150	Optimizing current conveyors by evolutionary algorithms including differential evolution. , 2009, , .		17
151	Characterization of Analog Circuits Using Transfer Function Trajectories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1796-1804.	5.4	17
152	A 16.1-bit Resolution 0.064-mm <sup>2</sup> Compact Highly Digital Closed-Loop Single-VCO-Based 1-1 Sturdy-MASH Resistance-to-Digital Converter With High Robustness in 180-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 2456-2467.	5.4	17
153	Analog routing for manufacturability. , 0, , .		16
154	Behavioral model of reusable D/A converters. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1323-1326.	2.2	16
155	A fast learning algorithm for time-delay neural networks. Information Sciences, 2002, 148, 27-39.	6.9	16
156	Hierarchical analog circuit reliability analysis using multivariate nonlinear regression and active learning sample selection. , 2012, , .		16
157	Recurrent sparse support vector regression machines trained by active learning in the time-domain. Expert Systems With Applications, 2012, 39, 10933-10942.	7.6	16
158	Optimization of analog fault coverage by exploiting defect-specific masking. , 2014, , .		16
159	Automated testing of mixed-signal integrated circuits by topology modification. , 2015, , .		16
160	Analog fault coverage improvement using final-test dynamic part average testing. , 2016, , .		16
161	Testing of analog integrated circuits based on power-supply current monitoring and discrimination analysis. , 0, , .		15
162	Mondriaan: a tool for automated layout synthesis of array-type analog blocks. , 0, , .		15

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163	Nonlinear behavioral modeling and phase noise evaluation in phase locked loops. , 0, , .		15
164	Symbolic analysis of large analog circuits using a sensitivity-driven enumeration of common spanning trees. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1342-1350.	2.2	15
165	A 14-bit 130-MHz CMOS current-steering DAC with adjustable INL. , 0, , .		15
166	A Monolithically Integrated On-Chip Antenna in 0.18 $\mu\text{m}$ Standard CMOS Technology for Far-Field Short-Range Wireless Powering. IEEE Antennas and Wireless Propagation Letters, 2010, 9, 631-633.	4.0	15
167	High-density optrode-electrode neural probe using SixNy photonics for in vivo optogenetics. , 2015, , .		15
168	A Robust BBPLL-Based 0.18- $\mu\text{m}$ CMOS Resistive Sensor Interface With High Drift Resilience Over a $40\text{ }^{\circ}\text{C}$ – $175\text{ }^{\circ}\text{C}$ Temperature Range. IEEE Journal of Solid-State Circuits, 2019, 54, 1862-1873.	5.4	15
169	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS?Part 2: Architectures and Circuits. IEEE Solid-State Circuits Magazine, 2020, 12, 18-27.	0.4	15
170	An intelligent design system for analogue integrated circuit. , 0, , .		14
171	A methodology for analog design automation in mixed-signal ASICs. , 0, , .		14
172	Analyzing the impact of substrate noise on embedded analog-to-digital converters. , 0, , .		14
173	NBTI model for analogue IC reliability simulation. Electronics Letters, 2010, 46, 1279.	1.0	14
174	Designing reliable analog circuits in an unreliable world. , 2012, , .		14
175	Novel Wire-Grid Nano-Antenna Array With Circularly Polarized Radiation for Wireless Optical Communication Systems. Journal of Lightwave Technology, 2017, 35, 4700-4706.	4.6	14
176	A novel method for the fault detection of analog integrated circuits. , 0, , .		14
177	DESIGN OF AN ENERGY-EFFICIENT PULSED UWB RECEIVER. , 2007, , 303-329.		14
178	EsteMate: a tool for automated power and area estimation in analog top-down design and synthesis. , 0, , .		13
179	High-level simulation of substrate noise in high-ohmic substrates with interconnect and supply effects. , 2004, , .		13
180	Generalized Simulation-Based Posynomial Model Generation for Analog Integrated Circuits. Analog Integrated Circuits and Signal Processing, 2004, 40, 193-203.	1.4	13

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181	Simulation-based optimization of UGCs performances. , 2008, , .		13
182	The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time $\Sigma\Delta$ Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 416-420.	3.0	13
183	Stochastic circuit reliability analysis. , 2011, , .		13
184	Towards a noise prediction model for in vivo neural recording. , 2012, 2012, 759-62.		13
185	An energy-efficient capacitance-controlled oscillator-based sensor interface for MEMS sensors. , 2013, , .		13
186	Symbolic approximation strategies and the symbolic analysis of large and nonlinear circuits. , 0, , .		12
187	Models for systematic design and verification of frequency synthesizers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1301-1308.	2.2	12
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