Yongxun Liu

List of Publications by Year in descending order

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143 papers	1,693 citations	361413 20 h-index	377865 34 g-index
143 all docs	143 docs citations	143 times ranked	1045 citing authors

#	Article	IF	Citations
1	Demonstration, Analysis, and Device Design Considerations for Independent DG MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 2046-2053.	3.0	115
2	A Highly Threshold Voltage-Controllable 4T FinFET with an 8.5-nm-Thick Si-Fin Channel. IEEE Electron Device Letters, 2004, 25, 510-512.	3.9	97
3	Investigation of the TiN Gate Electrode With Tunable Work Function and Its Application for FinFET Fabrication. IEEE Nanotechnology Magazine, 2006, 5, 723-730.	2.0	90
4	Ideal rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching. IEEE Electron Device Letters, 2003, 24, 484-486.	3.9	83
5	Variability Analysis of TiN Metal-Gate FinFETs. IEEE Electron Device Letters, 2010, 31, 546-548.	3.9	63
6	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
7	Ultrathin Channel Vertical DG MOSFET Fabricated by Using Ion-Bombardment-Retarded Etching. IEEE Transactions on Electron Devices, 2004, 51, 2078-2085.	3.0	50
8	Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. IEEE Electron Device Letters, 2007, 28, 517-519.	3.9	48
9	Cross-Sectional Channel Shape Dependence of Short-Channel Effects in Fin-Type Double-Gate Metal Oxide Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2004, 43, 2151-2155.	1.5	39
10	Fabrication of FinFETs by Damage-Free Neutral-Beam Etching Technology. IEEE Transactions on Electron Devices, 2006, 53, 1826-1833.	3.0	37
11	Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201.	2.4	35
12	On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs. , 2010, , .		32
13	Enhancing SRAM cell performance by using independent double-gate FinFET. , 2008, , .		30
14	Advanced FinFET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs. , 2006, , .		28
15	Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. IEEE Electron Device Letters, 2007, 28, 1123-1125.	3.9	28
16	Nanoscale Wet Etching of Physical-Vapor-Deposited Titanium Nitride and Its Application to Sub-30-nm-Gate-Length Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Fabrication. Japanese Journal of Applied Physics, 2010, 49, 06GH18.	1.5	27
17	Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010.	3.0	27
18	Independent-Double-Gate FinFET SRAM for Leakage Current Reduction. IEEE Electron Device Letters, 2009, 30, 757-759.	3.9	24

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19	A Comparative Study of Nitrogen Gas Flow Ratio Dependence on the Electrical Characteristics of Sputtered Titanium Nitride Gate Bulk Planar Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors and Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 05DC01.	1.5	23
20	Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness. IEEE Electron Device Letters, 2009, 30, 407-409.	3.9	23
21	Investigation of Low-Energy Tilted Ion Implantation for Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Extension Doping. Japanese Journal of Applied Physics, 2010, 49, 04DC18.	1.5	22
22	Suppressing V<inf>t</inf> and G<inf>m</inf> variability of FinFETs using amorphous metal gates for 14 nm and beyond. , 2012, , .		22
23	Systematic electrical characteristics of ideal rectangular cross section si-fin channel double-gate MOSFETs fabricated by a wet process. IEEE Nanotechnology Magazine, 2003, 2, 198-204.	2.0	21
24	Fin-Type Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistors Fabricated by Orientation-Dependent Etching and Electron Beam Lithography. Japanese Journal of Applied Physics, 2003, 42, 4142-4146.	1.5	21
25	FK506-protective effects against trimethyltin neurotoxicity in rats: Hippocampal expression analyses reveal the involvement of periarterial osteopontin. Neuroscience, 2008, 153, 1135-1145.	2.3	21
26	Nitrogen Gas Flow Ratio and Rapid Thermal Annealing Temperature Dependences of Sputtered Titanium Nitride Gate Work Function and Their Effect on Device Characteristics. Japanese Journal of Applied Physics, 2008, 47, 2433.	1.5	20
27	Experimental Study of Effective Carrier Mobility of Multi-Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors with (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching. Japanese Journal of Applied Physics, 2006, 45, 3084-3087.	1.5	18
28	Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation. IEEE Nanotechnology Magazine, 2007, 6, 201-205.	2.0	18
29	A thermomechanical relay with microspring contact array. , 0, , .		15
30	High density electrical feedthrough fabricated by deep reactive ion etching of Pyrex glass. , 0, , .		15
31	Variability Origins of Parasitic Resistance in FinFETs With Silicided Source/Drain. IEEE Electron Device Letters, 2012, 33, 474-476.	3.9	15
32	Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, .	3.3	15
33	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
34	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
35	Fin-Height Effect on Poly-Si/PVD-TiN Stacked-Gate FinFET Performance. IEEE Transactions on Electron Devices, 2012, 59, 647-653.	3.0	14
36	Fabrication of ultrathin Si Channel Wall For Vertical Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DG MOSFET) by Using Ion-Bombardment-Retarded Etching (IBRE). Japanese Journal of Applied Physics, 2003, 42, 1916-1918.	1.5	13

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37	Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology. , 2007, , .		13
38	Enhancement of FinFET performance using 25-nm-thin sidewall spacer grown by atomic layer deposition. Solid-State Electronics, 2012, 74, 13-18.	1.4	13
39	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	13
40	Work function controllability of metal gates made by interdiffusing metal stacks with low and high work functions. Microelectronic Engineering, 2005, 80, 284-287.	2.4	12
41	Optimum Gate Workfunction for $V_{m th}$-Controllable Four-Terminal-Driven Double-Gate MOSFETs (4T-XMOSFETs)â€"Band-Edge Workfunction Versus Midgap Workfunction. IEEE Nanotechnology Magazine, 2006, 5, 716-722.	2.0	12
42	Threshold-Voltage Reduction of FinFETs by Ta/Mo Interdiffusion Dual Metal-Gate Technology for Low-Operating-Power Application. IEEE Transactions on Electron Devices, 2008, 55, 2454-2461.	3.0	12
43	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n⁺-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€"Oxideâ€"Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	12
44	Variability Analysis of Scaled Crystal Channel and Poly-Si Channel FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 573-581.	3.0	12
45	Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11.	1.5	12
46	15-nm-thick Si channel wall vertical double-gate MOSFET. , 0, , .		11
47	Metal-Gate FinFET Variation Analysis by Measurement and Compact Model. IEEE Electron Device Letters, 2009, 30, 556-558.	3.9	11
48	Carrier injection by static induction mechanism in MLE-grown planar-doped barrier n/sup +/-i-p/sup +/-i-n/sup +/ structures. IEEE Transactions on Electron Devices, 1997, 44, 195-197.	3.0	10
49	Demonstration of Split-Gate Type Trigate Flash Memory With Highly Suppressed Over-Erase. IEEE Electron Device Letters, 2012, 33, 345-347.	3.9	10
50	An experimental study of solid source diffusion by spin on dopants and its application for minimal silicon-on-insulator CMOS fabrication. Japanese Journal of Applied Physics, 2017, 56, 06GG01.	1.5	10
51	Fabrication and characterization of vertical-type, self-aligned asymmetric double-gate metal-oxide-semiconductor field-effect-transistors. Applied Physics Letters, 2005, 86, 123512.	3.3	9
52	Fabrication of a Vertical-Channel Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor Using a Neutral Beam Etching. Japanese Journal of Applied Physics, 2006, 45, L279-L281.	1.5	9
53	A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. IEEE Electron Device Letters, 2007, 28, 452-454.	3.9	9
54	A Ta/Mo Interdiffusion Dual Metal Gate Technology for Drivability Enhancement of FinFETs. IEEE Electron Device Letters, 2008, 29, 618-620.	3.9	9

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55	Investigation of N-Channel Triple-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors on (100) Silicon On Insulator Substrate. Japanese Journal of Applied Physics, 2006, 45, 3097-3100.	1.5	8
56	Fin-height controlled TiN-gate FinFET CMOS based on experimental mobility. Microelectronic Engineering, 2007, 84, 2101-2104.	2.4	8
57	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. , 2008, , .		8
58	Atomic Layer Deposition of SiO₂ for the Performance Enhancement of Fin Field Effect Transistors. Japanese Journal of Applied Physics, 2013, 52, 116503.	1.5	8
59	Novel Process for Vertical Double-Gate (DG) Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) Fabrication. Japanese Journal of Applied Physics, 2003, 42, 4138-4141.	1.5	7
60	Damage-free neutral beam etching technology for high mobility FinFETs. , 0, , .		7
61	Fabrication and characterization of vertical-type double-gate metal-oxide-semiconductor field-effect transistor with ultrathin Si channel and self-aligned source and drain. Applied Physics Letters, 2006, 88, 072103.	3.3	7
62	Investigation of Thermal Stability of TiN Film Formed by Atomic Layer Deposition Using Tetrakis(dimethylamino)titanium Precursor for Metal-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 04DA16.	1.5	7
63	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	7
64	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7
65	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7
66	Electron beam lithography with negative tone resist for highly integrated silicon quantum bits. Nanotechnology, 2021, 32, 485301.	2.6	7
67	Impact of extension and source/drain resistance on FinFET performance. , 2008, , .		6
68	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	6
69	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
70	Investigation of piezoresistive effect in p-channel metalâ€“oxideâ€“semiconductor field-effect transistors fabricated on circular silicon-on-insulator diaphragms using cost-effective minimal-fab process. Japanese Journal of Applied Physics, 2018, 57, 06HD03.	1.5	6
71	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n+-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	6
72	Electron mobility in multi-FinFET with a (111) channel surface fabricated by orientation-dependent wet etching. Microelectronic Engineering, 2005, 80, 390-393.	2.4	5

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73	Demonstration and Analysis of Accumulation-Mode Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2006, 45, 3079-3083.	1.5	5
74	New Fabrication Technology of Fin Field Effect Transistors Using Neutral-Beam Etching. Japanese Journal of Applied Physics, 2006, 45, 5513-5516.	1.5	5
75	Comparative Study of Charge Trapping Type SOI-FinFET Flash Memories with Different Blocking Layer Materials. Journal of Low Power Electronics and Applications, 2014, 4, 153-167.	2.0	5
76	Robust and compact key generator using physically unclonable function based on logic-transistor-compatible poly-crystalline-Si channel FinFET technology. , 2015, , .		5
77	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
78	Demonstration of threshold voltage control techniques for vertical-type 4-terminal double-gate MOSFETs (4T-DGFET). , 0, , .		4
79	Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes. Japanese Journal of Applied Physics, 2007, 46, 1825-1829.	1.5	4
80	Vertical doubleâ€gate MOSFET device technology. Electronics and Communications in Japan, 2008, 91, 46-51.	0.5	4
81	Dual-Metal-Gate Transistors with Symmetrical Threshold Voltages Using Work-Function-Tuned Ta/Mo Bilayer Metal Gates. Japanese Journal of Applied Physics, 2008, 47, 2428-2432.	1.5	4
82	Enhancing Noise Margins of Fin-Type Field Effect Transistor Static Random Access Memory Cell by Using Threshold Voltage-Controllable Flexible-Pass-Gates. Applied Physics Express, 2009, 2, 054502.	2.4	4
83	Variability Analysis of TiN FinFET SRAM Cells and Its Compensation by Independent-DG FinFETs. IEEE Electron Device Letters, 2010, 31, 1095-1097.	3.9	4
84	Independent double-gate FinFET SRAM technology. , 2011, , .		4
85	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4
86	(Invited) Charge Trapping Type SOI-FinFET Flash Memory. ECS Transactions, 2014, 61, 263-280.	0.5	4
87	Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06.	1.5	4
88	Epitaxial growth of Ge thin film on Si (001) by DC magnetron sputtering. Materials Science in Semiconductor Processing, 2017, 70, 3-7.	4.0	4
89	Enhancing noise margins of FinFET SRAM by integrating V<inf>th</inf>-controllable flexible-pass-gates. , 2008, , .		3
90	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. Solid-State Electronics, 2009, 53, 701-705.	1.4	3

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91	Variability origins of FinFETs and perspective beyond 20nm node. , 2011, , .		3
92	A Correlative Analysis Between Characteristics of FinFETs and SRAM Performance. IEEE Transactions on Electron Devices, 2012, 59, 1345-1352.	3.0	3
93	Gate Structure Dependence of Variability in Polycrystalline Silicon Fin-Channel Flash Memories. Japanese Journal of Applied Physics, 2013, 52, 06GE01.	1.5	3
94	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
95	Impact of extension implantation conditions of fin field-effect transistors on gate-induced drain leakage. Japanese Journal of Applied Physics, 2016, 55, 04EB01.	1.5	3
96	Impact of residual defects caused by extension ion implantation in FinFETs on parasitic resistance and its fluctuation. Solid-State Electronics, 2017, 132, 103-108.	1.4	3
97	Tunneling through ultrathin GaAs n/sup ++/-p/sup ++/-n/sup ++/ barrier grown by molecular layer epitaxy. IEEE Transactions on Electron Devices, 1998, 45, 2551-2554.	3.0	2
98	Tunnelling currents in very thin planar-doped barrier n+-i-p+-i-n+ structures. IET Circuits, Devices and Systems, 1999, 146, 31.	0.6	2
99	P-Channel Vertical Double-Gate MOSFET Fabricated by Utilizing Ion-Bombardment-Retarded Etching Processs. Japanese Journal of Applied Physics, 2004, 43, 2156-2159.	1.5	2
100	Logic gate threshold voltage controllable single metal gate FinFET CMOS inverters implemented by using co-integration of 3T/4T-FinFETs. , 2008, , .		2
101	Experimental evaluation of parallel transmission using optical ZCZ-CDMA system. , 2009, , .		2
102	Vertical ultrathinâ€channel multiâ€gate MOSFETs (MuGFETs): technological challenges and future developments. IEEJ Transactions on Electrical and Electronic Engineering, 2009, 4, 386-391.	1.4	2
103	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	2
104	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	2
105	(Invited) FinFET Flash Memory Technology. ECS Transactions, 2012, 45, 289-310.	0.5	2
106	Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16.	1.5	2
107	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2
108	Fabrication of nano-capillary emitter arrays for ionic liquid electrospray thrusters. Japanese Journal of Applied Physics, 2021, 60, SCCF07.	1.5	2

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109	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	2
110	Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04.	1.5	2
111	FinFET-Based Flex-Vth SRAM Design for Drastic Standby-Leakage-Current Reduction. IEICE Transactions on Electronics, 2008, E91-C, 534-542.	0.6	2
112	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	2
113	Tunnelling current analysis of GaAs n++-p++-n++ ultrathin barrier structures grown by molecular layer epitaxy. IET Circuits, Devices and Systems, 1999, 146, 218.	0.6	1
114	Device Design Consideration forVth-Controllable Four-Terminal Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2005, 44, 2351-2356.	1.5	1
115	Flex-pass-gate SRAM for static noise margin enhancement using FinFET-based technology. Solid-State Electronics, 2008, 52, 1694-1702.	1.4	1
116	Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction. , 2008, , .		1
117	(Invited) Advanced FinFET Technologies: Extension Doping, Vth Controllable CMOS Inverters and SRAM. ECS Transactions, 2010, 28, 385-401.	0.5	1
118	Correlative analysis between characteristics of 30-nm L<inf>G</inf> FinFETs and SRAM performance. , 2011, , .		1
119	Fabrication of PVD-TiN metal-gate SOI-CMOS integrated circuits using minimal-fab and mega-fab hybrid process. , 2016, , .		1
120	(Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24.	0.5	1
121	Process development for CMOS fabrication using minimal fab. , 2017, , .		1
122	High-Frequency Precise Characterization of Intrinsic FinFET Channel. IEICE Transactions on Electronics, 2012, E95.C, 752-760.	0.6	1
123	Impact ionisation in GaAs planar-doped barrier structures grown by molecular layer epitaxy. IET Circuits, Devices and Systems, 2000, 147, 165.	0.6	1
124	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	1
125	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	1
126	Independent-Double-Gate FinFET SRAM Technology. IEICE Transactions on Electronics, 2013, E96.C, 413-423.	0.6	1

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127	Emerging double-gate FinFETs technology. , 0, , .		0
128	Flexible threshold voltage 4-terminal FinFETs. , 0, , .		0
129	On the V/sub th/ controllability for 4-terminal double-gate MOSFETs. , 0, , .		0
130	Work function control of metal gates by interdiffused Ni-Ta with high thermal stability. , 0, , .		0
131	Nitrogen gas flow ratio controlled PVD TiN metal gate technology for FinFET CMOS. , 2007, , .		0
132	Variable-Threshold-Voltage FinFETs with a Control-Voltage Range within the Logic-Level Swing Using Asymmetric Work-Function Double Gates. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	0
133	Minimization of Gate-Induced Drain Leakage by Controlling Gate Underlap Length for Low-Standby-Power Operation of 20-nm-Level Four-Terminal Silicon-on-Insulator Fin-Shaped Field Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 024203.	1.5	0
134	Variability analysis of TiN FinFET SRAM cell performance and its compensation using Vth-controllable independent double-gate FinFET. , 2010, , .		0
135	Static noise margin enhancement by flex-pass-gate SRAM. Electronics and Communications in Japan, 2011, 94, 57-64.	0.5	0
136	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	0
137	(Invited) On-Current Variability Sources of FinFETs: Analysis and Perspective for 14nm-Lg Technology. ECS Transactions, 2012, 45, 231-242.	0.5	0
138	1/fNoise Characteristics of Fin-Type Field-Effect Transistors in Saturation Region. Japanese Journal of Applied Physics, 2013, 52, 04CC23.	1.5	0
139	Experimental study of charge trapping type FinFET flash memory. , 2014, , .		0
140	Highly Vt tunable and low variability triangular fin-channel MOSFETs on SOTB. Microelectronic Engineering, 2015, 147, 290-293.	2.4	0
141	Structural and electrical characterization of epitaxial Ge thin films on Si(001) formed by sputtering. Japanese Journal of Applied Physics, 2017, 56, 04CB01.	1.5	0
142	Independent-Double-Gate FINFET SRAM Cell for Drastic Leakage Current Reduction. Lecture Notes in Electrical Engineering, 2010, , 67-79.	0.4	0
143	A 0.7-V Opamp in Scaled Low-Standby-Power FinFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 686-695.	0.6	0