Koichi Fukuda

List of Publications by Year
in descending order

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81	749	687363 13	794594 19
papers	citations	h-index	g-index

81	81	81	633
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Cellular automaton approach for carrier degeneracy effects on the electron mobility of high electron mobility transistors. Japanese Journal of Applied Physics, 2022, 61, SC1043.	1.5	0
2	Importance of source and drain extension design in cryogenic MOSFET operation: causes of unexpected threshold voltage increases. Applied Physics Express, 2022, 15, 084004.	2.4	2
3	A Poissonâ€“Schrodinger and cellular automaton coupled approach for two-dimensional electron gas transport modeling of GaN-based high mobility electron transistors. Japanese Journal of Applied Physics, 2021, 60, SBBD04.	1.5	3
4	Improved Channel Electron Mobility Through Electric Field Reduction in GaN Quantum-Well Double-Heterostructures. IEEE Electron Device Letters, 2021, 42, 1592-1595.	3.9	5
5	Technology computer-aided design simulation of phonon heat transport in semiconductor devices. Japanese Journal of Applied Physics, 2021, 60, SBBA03.	1.5	4
6	Si bilayer tunnel field-effect transistor structure realized using tilted ion-implantation technique. Solid-State Electronics, 2021, 180, 107993.	1.4	2
7	Buried nanomagnet realizing high-speed/low-variability silicon spin qubits: implementable in error-correctable large-scale quantum computers. , 2021, , .		1
8	Temperature-dependent mobility modeling of GaN HEMTs by cellular automaton method. , 2021, , .		0
9	Theoretical analysis of photo-recycling effect on external quantum efficiency considering spatial carrier dynamics. Japanese Journal of Applied Physics, 2020, 59, SGGK02.	1.5	0
10	Circuit speed oriented device design scheme for GaAsSb/InGaAs double-gate hetero-junction tunnel FETs. Japanese Journal of Applied Physics, 2020, 59, SGGA06.	1.5	2
11	Device simulation of negative-capacitance field-effect transistors with a uniaxial ferroelectric gate insulator. Nonlinear Theory and Its Applications IEICE, 2020, 11, 145-156.	0.6	1
12	Implementation of Coulomb blockade transport on a semiconductor device simulator and its application to tunnel-FET-based quantum dot devices. Japanese Journal of Applied Physics, 2020, 59, SIIE02.	1.5	2
13	Novel multi-flux semiconductor device simulation method applied to 2DEG analyzes. Japanese Journal of Applied Physics, 2020, 59, SGGA05.	1.5	0
14	Mechanism of extraordinary gate-length dependence of quantum dot operation in isoelectronic-trap-assisted tunnel FETs. Applied Physics Express, 2020, 13, 114001.	2.4	1
15	Theoretical Formulation of Experimentally Observed Quantum Efficiency ofÂRadiation in Semiconducting Crystal. Physical Review Applied, 2019, 12, .	3.8	3
16	Implementation of Automatic Differentiation to Python-based Semiconductor Device Simulator. , 2019, , .		1
17	Simulation of deep level transient spectroscopy using circuit simulator with deep level trap model implemented by Verilog-A language. , 2019, , .		0
18	Steep switching less than 15 mV dec^{â^'1} in silicon-on-insulator tunnel FETs by a trimmed-gate structure. Japanese Journal of Applied Physics, 2019, 58, SBBA16.	1.5	8

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19	A time-dependent Verilog-A compact model for MOS capacitors with interface traps. Japanese Journal of Applied Physics, 2019, 58, SBBD06.	1.5	1
20	A TCAD device simulator for exotic materials and its application to a negative-capacitance FET. Journal of Computational Electronics, 2019, 18, 534-542.	2.5	19
21	Process and device integration for silicon tunnel FETs utilizing isoelectronic trap technology to enhance the ON current. Japanese Journal of Applied Physics, 2018, 57, 04FA04.	1.5	4
22	Simulation study of short-channel effects of tunnel field-effect transistors. Japanese Journal of Applied Physics, 2018, 57, 04FD04.	1.5	3
23	Design of steep-slope negative-capacitance FinFETs for dense integration: Importance of appropriate ferroelectric capacitance and short-channel effects. Japanese Journal of Applied Physics, 2018, 57, 04FD03.	1.5	2
24	Fringing field effects in negative capacitance field-effect transistors with a ferroelectric gate insulator. Japanese Journal of Applied Physics, 2018, 57, 04FD07.	1.5	16
25	A transient simulation approach to obtaining capacitanceâ€“voltage characteristics of GaN MOS capacitors with deep-level traps. Japanese Journal of Applied Physics, 2018, 57, 04FG04.	1.5	3
26	Multidomain Dynamics of Ferroelectric Polarization and its Coherency-Breaking in Negative Capacitance Field-Effect Transistors. , 2018, , .		9
27	Device Simulation of Negative-Capacitance Field-Effect Transistors With a Ferroelectric Gate Insulator. , 2018, , .		3
28	Steep switching in trimmed-gate tunnel FET. AIP Advances, 2018, 8, .	1.3	5
29	Enhancement of capacitance benefit by drain offset structure in tunnel field-effect transistor circuit speed associated with tunneling probability increase. Japanese Journal of Applied Physics, 2018, 57, 04FD13.	1.5	1
30	On the drain bias dependence of long-channel silicon-on-insulator-based tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD04.	1.5	2
31	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
32	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2
33	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
34	Perspective of negative capacitance FinFETs investigated by transient TCAD simulation. , 2017, , .		17
35	Structural advantages of silicon-on-insulator FETs over FinFETs in steep subthreshold-swing operation in ferroelectric-gate FETs. Japanese Journal of Applied Physics, 2017, 56, 04CD10.	1.5	9
36	Simulation of GaN MOS capacitance with frequency dispersion and hysteresis. , 2017, , .		0

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37	Interlayer coupling effect on the performance of monolithic three-dimensional inverters and its dependence on the interlayer dielectric thickness. Japanese Journal of Applied Physics, 2017, 56, 04CC02.	1.5	4
38	Compact model of ferroelectric-gate field-effect transistor for circuit simulation based on multidomain Landauâ€“Kalathnikov theory. Japanese Journal of Applied Physics, 2017, 56, 04CE07.	1.5	7
39	Design and simulation of steep-slope silicon-on-insulator FETs using negative capacitance: Impact of buried oxide thickness and remnant polarization. , 2016, , .		1
40	Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration. , 2016, , .		77
41	Material and device engineering in fully depleted silicon-on-insulator transistors to realize a steep subthreshold swing using negative capacitance. Japanese Journal of Applied Physics, 2016, 55, 08PD01.	1.5	20
42	Scaling limit for InGaAs/GaAsSb heterojunction double-gate tunnel FETs from the viewpoint of direct band-to-band tunneling from source to drain induced off-characteristics deterioration. Japanese Journal of Applied Physics, 2016, 55, 070303.	1.5	3
43	Steep subthreshold swing and energy efficiency in MOSFFETs utilizing nonlinear gate dielectric insulators. Japanese Journal of Applied Physics, 2016, 55, 04ED02.	1.5	2
44	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
45	Closed-form analytical model of static noise margin for ultra-low voltage eight-transistor tunnel FET static random access memory. Japanese Journal of Applied Physics, 2016, 55, 04ED06.	1.5	4
46	Spatial variation of the work function in nano-crystalline TiN films measured by dual-mode scanning tunneling microscopy. Japanese Journal of Applied Physics, 2015, 54, 04DA03.	1.5	14
47	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7
48	Design guidelines to achieve minimum energy operation for ultra low voltage tunneling FET logic circuits. Japanese Journal of Applied Physics, 2015, 54, 04DC04.	1.5	15
49	A moving mesh method for device simulation. , 2015, , .		0
50	Effect of hot implantation on ON-current enhancement utilizing isoelectronic trap in Si-based tunnel field-effect transistors. Applied Physics Express, 2015, 8, 036503.	2.4	9
51	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
52	Study of gate leakage current paths in p-channel tunnel field-effect transistor by current separation measurement and device simulation. Japanese Journal of Applied Physics, 2015, 54, 034202.	1.5	1
53	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
54	Study of tunneling transport in Si-based tunnel field-effect transistors with ON current enhancement utilizing isoelectronic trap. Applied Physics Letters, 2015, 106, .	3.3	54

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55	Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201.	2.4	35
56	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4
57	Band-to-band tunneling current enhancement utilizing isoelectronic trap and its application to TFETs. , 2014, , .		22
58	Three-dimensional simulation of scanning tunneling microscopy for semiconductor carrier and impurity profiling. Journal of Applied Physics, 2014, 116, 023701.	2.5	4
59	Simulation of light-illuminated STM measurements. , 2014, , .		1
60	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
61	Predictivity of the non-local BTBT model for structure dependencies of tunnel FETs. , 2014, , .		9
62	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7
63	A compact model for tunnel field-effect transistors incorporating nonlocal band-to-band tunneling. Journal of Applied Physics, 2013, 114, 144512.	2.5	25
64	Quantitative Evaluation of Dopant Concentration in Shallow Silicon pâ€“n Junctions by Tunneling Current Mapping with Multimode Scanning Probe Microscopy. Japanese Journal of Applied Physics, 2013, 52, 04CA04.	1.5	5
65	Tunnel Field-Effect Transistor with Epitaxially Grown Tunnel Junction Fabricated by Source/Drain-First and Tunnel-Junction-Last Processes. Japanese Journal of Applied Physics, 2013, 52, 04CC25.	1.5	16
66	Spatial Distribution of Photocurrent in Si Stripes under Tilted Illumination Measured by Multimode Scanning Probe Microscopy. Japanese Journal of Applied Physics, 2012, 51, 088005.	1.5	6
67	Radiation Resistance of SOI Pixel Devices Fabricated With OKI 0.15 $mu {m m}$ FD-SOI Technology. IEEE Transactions on Nuclear Science, 2009, 56, 2896-2904.	2.0	19
68	Analysis of temperature and process variation effects on photo sensor circuits using device/circuit mixed-mode simulations. , 2008, , .		1
69	Ion implantation model for channeling through multi-layers. , 2008, , .		1
70	Random telegraph noise in flash memories - model and technology scaling. , 2007, , .		95
71	SOI pixel developments in a 0.15μm technology. , 2007, , .		5
72	R&D of a pixel sensor based on fully depleted SOI technology. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2007, 582, 861-865.	1.6	10

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73	Monolithic Pixel Detector in a 0.15 μm SOI Technology. , 2006, , .		12
74	ESD Protection Design Optimization Using a Mixed-Mode Simulation and Its Impact on ESD Protection Design of Power Bus Line Resistance. , 2005, , .		9
75	An interpolated flux scheme for cellular automaton device simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 553-560.	2.7	5
76	A device simulation of the BBT effect in flash memory cells and implications for the development of highâ€reliability memory cells. Electronics and Communications in Japan, 1996, 79, 51-57.	0.2	0
77	Technology CAD at OKI. Microelectronics Journal, 1995, 26, 159-175.	2.0	5
78	New Efficient Treatment of Impact Ionization in Submicron Metal-Oxide-Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 1992, 31, 3763-3769.	1.5	1
79	Channel dopant profile and Leff extraction of deep submicron MOSFETs by inverse modeling. , 0, , .		0
80	Application of TCAD to designing advanced DRAM and logic devices. , 0, , .		2
81	Undoped Thin Film FD-SOI CMOS with Source/Drain-to-Gate Non-overlapped Structure for Ultra Low Leak Applications. , 0, , .		4