Nikil Dutt

List of Publications by Year
in descending order

376 papers	6,230 citations	201674 27 h-index	214800 47 g-index
394 all docs	394 docs citations	394 times ranked	3441 citing authors

#	Article	IF	Citations
1	Fast exploration of bus-based communication architectures at the CCATB abstraction. Transactions on Embedded Computing Systems, 2008, 7, 1-32.	2.9	311
2	EXPRESSION. , 1999, , .		295
3	A configurable simulation environment for the efficient simulation of large-scale spiking neural networks on graphics processors. Neural Networks, 2009, 22, 791-800.	5.9	168
4	Reliable on-chip systems in the nano-era. , 2013, , .		156
5	Memory Issues in Embedded Systems-on-Chip. , 1999, , .		135
6	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 8-23.	2.7	125
7	Post-Quantum Lattice-Based Cryptography Implementations. ACM Computing Surveys, 2019, 51, 1-41.	23.0	123
8	HiCH. Transactions on Embedded Computing Systems, 2017, 16, 1-20.	2.9	118
9	Sleep Tracking of a Commercially Available Smart Ring and Smartwatch Against Medical-Grade Actigraphy in Everyday Settings: Instrument Validation Study. JMIR MHealth and UHealth, 2020, 8, e20465.	3.7	76
10	Physically-aware HW-SW partitioning for reconfigurable architectures with partial dynamic reconfiguration. , 2005, , .		73
11	Instruction set compiled simulation. , 2003, , .		72
12	SPARTA. , 2016, , .		71
13	Toward Smart Embedded Systems. Transactions on Embedded Computing Systems, 2016, 15, 1-27.	2.9	71
14	Neural correlates of sparse coding and dimensionality reduction. PLoS Computational Biology, 2019, 15, e1006908.	3.2	71
15	Partitioned register files for VLIWs. ACM SIGMICRO Newsletter, 1992, 23, 292-300.	0.4	69
16	CARLsim 4: An Open Source Library for Large Scale, Biologically Detailed Spiking Neural Network Simulation using Heterogeneous Clusters. , 2018, , .		69
17	Extending the transaction level modeling approach for fast communication architecture exploration. , 2004, , .		61
18	Integrated power management for video streaming to mobile handheld devices. , 2003, , .		59

#	Article	IF	Citations
19	Efficient simulation of large-scale Spiking Neural Networks using CUDA graphics processors. , 2009, , .		58
20	An efficient automated parameter tuning framework for spiking neural networks. Frontiers in Neuroscience, 2014, 8, 10.	2.8	56
21	Fast exploration of bus-based on-chip communication architectures. , 2004, , .		55
22	Unsupervised heart-rate estimation in wearables with Liquid states and a probabilistic readout. Neural Networks, 2018, 99, 134-147.	5.9	55
23	Exploiting Partially-Forgetful Memories for Approximate Computing. IEEE Embedded Systems Letters, 2015, 7, 19-22.	1.9	54
24	An Efficient Simulation Environment for Modeling Large-Scale Cortical Processing. Frontiers in Neuroinformatics, 2011, 5, 19.	2.5	53
25	A Real-time PPG Quality Assessment Approach for Healthcare Internet-of-Things. Procedia Computer Science, 2019, 151, 551-558.	2.0	51
26	Floorplan-aware automated synthesis of bus-based communication architectures. , 2005, , .		50
27	DYNAMO: A Cross-Layer Framework for End-to-End QoS and Energy Optimization in Mobile Handheld Devices. IEEE Journal on Selected Areas in Communications, 2007, 25, 722-737.	14.0	50
28	Mitigating soft error failures for multimedia applications by selective data protection. , 2006, , .		48
29	DRDU. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 15.	2.6	45
30	Introduction of local memory elements in instruction set extensions. , 2004, , .		44
31	ISEGEN: Generation of High-Quality Instruction Set Extensions by Iterative Improvement. , 0, , .		44
32	Self-awareness in remote health monitoring systems using wearable electronics. , 2017, , .		43
33	Functional abstraction driven design space exploration of heterogeneous programmable architectures. , 2001, , .		42
34	Compilation techniques for energy reduction in horizontally partitioned cache architectures. , 2005, , .		42
35	Dynamic backlight adaptation for low-power handheld devices. IEEE Design and Test of Computers, 2004, 21, 398-405.	1.0	41
36	Objective stress monitoring based on wearable sensors in everyday settings. Journal of Medical Engineering and Technology, 2020, 44, 177-189.	1.4	41

#	Article	IF	Citations
37	Memory aware compilation through accurate timing extraction. , 2000, , .		40
38	CARLsim 3: A user-friendly and highly optimized library for the creation of neurobiologically detailed spiking neural networks. , 2015, , .		40
39	Resilient dependable cyber-physical systems: a middleware perspective. Journal of Internet Services and Applications, 2012, 3, 41-49.	2.1	36
40	Personalized Maternal Sleep Quality Assessment: An Objective IoT-based Longitudinal Study. IEEE Access, 2019, 7, 93433-93447.	4.2	36
41	Long-Term IoT-Based Maternal Monitoring: System Design and Evaluation. Sensors, 2021, 21, 2281.	3.8	36
42	Fast configurable-cache tuning with a unified second-level cache. , 2005, , .		35
43	Self-Awareness in Systems on Chipâ€" A Survey. IEEE Design and Test, 2017, 34, 8-26.	1.2	35
44	A Cross-Layer Approach for Power-Performance Optimization in Distributed Mobile Systems. , 0, , .		33
45	Multiprocessor system-on-chip data reuse analysis for exploring customized memory hierarchies. , 2006, , .		33
46	Quality-Based Backlight Optimization for Video Playback on Handheld Devices. Advances in Multimedia, 2007, 2007, 1-10.	0.4	33
47	ORB: An on-chip optical ring bus communication architecture for multi-processor systems-on-chip. , 2008, , .		33
48	3D Visual Response Properties of MSTd Emerge from an Efficient, Sparse Population Code. Journal of Neuroscience, 2016, 36, 8399-8415.	3.6	32
49	SPECTR. , 2018, , .		32
50	Thermal-Aware Task Mapping on Dynamically Reconfigurable Network-on-Chip Based Multiprocessor System-on-Chip. IEEE Transactions on Computers, 2018, 67, 1818-1834.	3.4	32
51	System-level power-performance trade-offs in bus matrix communication architecture synthesis. , 2006, , .		31
52	A Multi-Granularity Power Modeling Methodology for Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 668-681.	3.1	31
53	Bypass aware instruction scheduling for register file power reduction. , 2006, , .		31
54	An efficient retargetable framework for instruction-set simulation. , 2003, , .		30

#	Article	IF	Citations
55	Specification-driven directed test generation for validation of pipelined processors. ACM Transactions on Design Automation of Electronic Systems, 2008, 13, 1-36.	2.6	30
56	Trends in Emerging On-Chip Interconnect Technologies. IPSJ Transactions on System LSI Design Methodology, 2008, 1, 2-17.	0.8	30
57	Efficient instruction encoding for automatic instruction set design of configurable ASIPs. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2002, , .	0.0	28
58	Efficient search space exploration for HW-SW partitioning. , 2004, , .		28
59	Constraint-driven bus matrix synthesis for MPSoC. , 2006, , .		28
60	E < MC2. , 2010, , .		28
61	A GPU-accelerated cortical neural network model for visually guided robot navigation. Neural Networks, 2015, 72, 75-87.	5.9	28
62	Pain Assessment Tool With Electrodermal Activity for Postoperative Patients: Method Validation Study. JMIR MHealth and UHealth, 2021, 9, e25258.	3.7	28
63	Speculation techniques for high level synthesis of control intensive designs. , 2001, , .		26
64	FFT-cache. , 2011, , .		26
65	APEX. , 2001, , .		25
66	Biologically plausible models of homeostasis and STDP: Stability and learning in spiking neural networks. , 2013, , .		25
67	Power / Capacity Scaling. , 2014, , .		25
68	Modeling and validation of pipeline specifications. Transactions on Embedded Computing Systems, 2004, 3, 114-139.	2.9	24
69	Energy-aware cosynthesis of real-time multimedia applications on MPSoCs using heterogeneous scheduling policies. Transactions on Embedded Computing Systems, 2008, 7, 1-19.	2.9	24
70	Optimal register assignment to loops for embedded code generation. ACM Transactions on Design Automation of Electronic Systems, 1996, 1, 251-279.	2.6	23
71	Hybrid-compiled simulation. Transactions on Embedded Computing Systems, 2009, 8, 1-27.	2.9	23
72	An Efficient and Robust Deep Learning Method with 1-D Octave Convolution to Extract Fetal Electrocardiogram. Sensors, 2020, 20, 3757.	3.8	23

#	Article	IF	Citations
73	Endurance-Aware Mapping of Spiking Neural Networks to Neuromorphic Hardware. IEEE Transactions on Parallel and Distributed Systems, 2022, 33, 288-301.	5.6	23
74	SOSA. , 2019, , .		23
75	A retargetable framework for instruction-set architecture simulation. Transactions on Embedded Computing Systems, 2006, 5, 431-452.	2.9	22
76	HaVOC. , 2012, , .		22
77	Neural and Synaptic Array Transceiver: A Brain-Inspired Computing Framework for Embedded Learning. Frontiers in Neuroscience, 2018, 12, 583.	2.8	22
78	pyEDA: An Open-Source Python Toolkit for Pre-processing and Feature Extraction of Electrodermal Activity. Procedia Computer Science, 2021, 184, 99-106.	2.0	22
79	Architecture description language (ADL)-driven software toolkit generation for architectural exploration of programmable SOCs. ACM Transactions on Design Automation of Electronic Systems, 2006, 11, 626-658.	2.6	21
80	Integrated Kernel Partitioning and Scheduling for Coarse-Grained Reconfigurable Arrays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1803-1816.	2.7	21
81	A Framework to Explore Workload-Specific Performance and Lifetime Trade-offs in Neuromorphic Computing. IEEE Computer Architecture Letters, 2019, 18, 149-152.	1.5	21
82	Operation tables for scheduling in the presence of incomplete bypassing. , 2004, , .		20
83	Mitigating the impact of hardware defects on multimedia applications. , 2008, , .		20
84	xTune. Transactions on Embedded Computing Systems, 2012, 11, 1-23.	2.9	20
85	Platform-Centric Self-Awareness as a Key Enabler for Controlling Changes in CPS. Proceedings of the IEEE, 2018, 106, 1543-1567.	21.3	20
86	CryptoPIM: In-memory Acceleration for Lattice-based Cryptographic Hardware. , 2020, , .		20
87	Investigation of Machine Learning Approaches for Traumatic Brain Injury Classification via EEG Assessment in Mice. Sensors, 2020, 20, 2027.	3.8	20
88	Synthesis of On-Chip Communication Architectures. , 2008, , 185-252.		20
89	Low power address encoding using self-organizing lists. , 2001, , .		19
90	ARGO: Aging-aware GPGPU register file allocation. , 2013, , .		19

#	Article	IF	Citations
91	Mechanisms underlying the basal forebrain enhancement of topâ€down and bottomâ€up attention. European Journal of Neuroscience, 2014, 39, 852-865.	2.6	19
92	A top-down methodology for microprocessor validation. IEEE Design and Test of Computers, 2004, 21, 122-131.	1.0	18
93	Analytical models for leakage power estimation of memory array structures. , 2004, , .		18
94	Design space exploration of real-time multi-media MPSoCs with heterogeneous scheduling policies. , 2006, , .		18
95	Performance estimation of distributed real-time embedded systems by discrete event simulations. , 2007, , .		18
96	ViPZonE. , 2012, , .		18
97	Pain Recognition With Electrocardiographic Features in Postoperative Patients: Method Validation Study. Journal of Medical Internet Research, 2021, 23, e25079.	4.3	18
98	FORAY-GEN: Automatic Generation of Affine Functions for Memory Optimizations. , 0, , .		17
99	PBExplore: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors. , 0, , .		17
100	Data reuse driven energy-aware MPSoC co-synthesis of memory and communication architecture for streaming applications. , 2006, , .		17
101	Exploring Energy Efficient Quantum-resistant Signal Processing Using Array Processors. , 2020, , .		17
102	Memory optimal single appearance schedule with dynamic loop count for synchronous dataflow graphs. , 2006, , .		16
103	Compilation framework for code size reduction using reduced bit-width ISAs (rISAs). ACM Transactions on Design Automation of Electronic Systems, 2006, 11, 123-146.	2.6	16
104	A large-scale neural network model of the influence of neuromodulatory levels on working memory and behavior. Frontiers in Computational Neuroscience, 2013, 7, 133.	2.1	16
105	Self-aware Cyber-Physical Systems-on-Chip. , 2015, , .		16
106	HiCAP. , 2016, , .		16
107	Generic Pipelined Processor Modeling and High Performance Cycle-Accurate Simulator Generation. , 0, , .		15
108	PARLGRAN. , 2006, , .		15

#	Article	IF	Citations
109	HESSLE-FREE. Transactions on Embedded Computing Systems, 2019, 18, 1-19.	2.9	15
110	Enabling Resource-Aware Mapping of Spiking Neural Networks via Spatial Decomposition. IEEE Embedded Systems Letters, 2021, 13, 142-145.	1.9	15
111	Memory Systems and Compiler Support for MPSoC Architectures. , 2005, , 251-281.		15
112	Personalized Stress Monitoring using Wearable Sensors in Everyday Settings. , 2021, 2021, 7332-7335.		15
113	Constraint-driven bus matrix synthesis for MPSoC. , 0, , .		14
114	Register File Power Reduction Using Bypass Sensitive Compiler. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1155-1159.	2.7	14
115	Quality-aware mobile graphics workload characterization for energy-efficient DVFS design. , 2014, , .		14
116	Run-DMC: Runtime dynamic heterogeneous multicore performance and power estimation for energy efficiency. , 2015, , .		14
117	Large-Scale Spiking Neural Networks using Neuromorphic Hardware Compatible Models. ACM Journal on Emerging Technologies in Computing Systems, 2015, 11, 1-18.	2.3	14
118	Approximation knob. , 2016, , .		14
119	Goal-Driven Autonomy for Efficient On-chip Resource Management: Transforming Objectives to Goals. , 2019, , .		14
120	Energy-efficient and Reliable Wearable Internet-of-Things through Fog-Assisted Dynamic Goal Management. Procedia Computer Science, 2019, 151, 493-500.	2.0	14
121	An Edge-Assisted and Smart System for Real-Time Pain Monitoring. , 2019, , .		14
122	A Probabilistic Formal Analysis Approach to Cross Layer Optimization in Distributed Embedded Systems. Lecture Notes in Computer Science, 2007, , 285-300.	1.3	14
123	PBPAIR. Mobile Computing and Communications Review, 2006, 10, 58-69.	1.7	14
124	Interface synthesis using memory mapping for an FPGA platform. , 0, , .		13
125	Processor-memory coexploration using an architecture description language. Transactions on Embedded Computing Systems, 2004, 3, 140-162.	2.9	13
126	Aggregating processor free time for energy reduction. , 2005, , .		13

#	Article	IF	Citations
127	Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1376-1380.	3.1	13
128	PTL: PCM Translation Layer. , 2012, , .		13
129	FPGA emulation and prototyping of a cyberphysical-system-on-chip (CPSoC). , 2014, , .		13
130	Multi-Layer Memory Resiliency. , 2014, , .		13
131	QuARK: Quality-configurable approximate STT-MRAM cache by fine-grained tuning of reliability-energy knobs. , 2017, , .		13
132	NeuroXplorer 1.0: An Extensible Framework for Architectural Exploration with Spiking Neural Networks. , 2021, , .		13
133	Minimization of memory traffic in high-level synthesis. , 1994, , .		12
134	Formal performance evaluation of AMBA-based system-on-chip designs. , 2006, , .		12
135	Cross-layer virtual observers for embedded multiprocessor system-on-chip (MPSoC). , 2012, , .		12
136	Models, abstractions, and architectures. , 2015, , .		12
137	Trends, challenges and needs for lattice-based cryptography implementations. , 2017, , .		12
138	Edge-Assisted Sensor Control in Healthcare IoT. , 2018, , .		12
139	Assessing the Mental Health of Emerging Adults Through a Mental Health App: Protocol for a Prospective Pilot Study. JMIR Research Protocols, 2021, 10, e25775.	1.0	12
140	DPCS. Transactions on Architecture and Code Optimization, 2015, 12, 1-26.	2.0	12
141	Co-Cap. , 2016, , .		12
142	Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions. IFIP Advances in Information and Communication Technology, 2002, , 81-90.	0.7	12
143	Quality Adapted Backlight Scaling (QABS) for Video Streaming to Mobile Handheld Devices. Lecture Notes in Computer Science, 2005, , 662-671.	1.3	11
144	Partially Protected Caches to Reduce Failures Due to Soft Errors in Multimedia Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1343-1347.	3.1	11

#	Article	IF	Citations
145	Memory-aware cooperative CPU-GPU DVFS governor for mobile games. , 2015, , .		11
146	ML-Gov. , 2017, , .		11
147	Interconnect-Aware Mapping of Applications to Coarse-Grain Reconfigurable Architectures. Lecture Notes in Computer Science, 2004, , 891-899.	1.3	11
148	Single appearance schedule with dynamic loop count for minimum data buffer from synchronous dataflow graphs. , 2005, , .		11
149	Compiler driven data layout optimization for regular/irregular array access patterns. , 2008, , .		11
150	Dynamic common sub-expression elimination during scheduling in high-level synthesis. , 2002, , .		10
151	Bypass aware instruction scheduling for register file power reduction. ACM SIGPLAN Notices, 2006, 41, 173-181.	0.2	10
152	System level power estimation methodology with H.264 decoder prediction IP case study. , 2007, , .		10
153	STEFAL: A System Level Temperature- and Floorplan-Aware Leakage Power Estimator for SoCs. , 2007, , .		10
154	NSF expedition on variability-aware software: Recent results and contributions. IT - Information Technology, 2015, 57, 181-198.	0.9	10
155	Self-Awareness in Cyber-Physical Systems. , 2016, , .		10
156	Synergistic CPU-GPU Frequency Capping for Energy-Efficient Mobile Games. Transactions on Embedded Computing Systems, 2018, 17, 1-24.	2.9	10
157	A Recurrent Neural Network Based Model of Predictive Smooth Pursuit Eye Movement in Primates. , 2018, , .		10
158	Gain scheduled control for nonlinear power management in CMPs. , 2018, , .		10
159	Approximation-aware coordinated power/performance management for heterogeneous multi-cores. , 2018, , .		10
160	ARGA. , 2019, , .		10
161	Dynamic Computation Migration at the Edge. , 2019, , .		10
162	CAST: Content-Aware STT-MRAM Cache Write Management for Different Levels of Approximation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4385-4398.	2.7	10

#	Article	IF	Citations
163	Edge-Assisted Control for Healthcare Internet of Things. ACM Transactions on Internet of Things, 2021, 2, 1-21.	4.6	10
164	Exploring computation offloading in IoT systems. Information Systems, 2022, 107, 101860.	3.6	10
165	Prospective Study Evaluating a Pain Assessment Tool in a Postoperative Environment: Protocol for Algorithm Testing and Enhancement. JMIR Research Protocols, 2020, 9, e17783.	1.0	10
166	CAPPS: A Framework for Powerâ€“Performance Tradeoffs in Bus-Matrix-Based On-Chip Communication Architecture Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 209-221.	3.1	9
167	REMEDIATE: A scalable fault-tolerant architecture for low-power NUCA cache in tiled CMPs. , 2013, , .		9
168	VAWOM. , 2013, , .		9
169	Conquering MPSoC complexity with principles of a self-aware information processing factory. , 2016, , .		9
170	CHIPS-AHOy. , 2018, , .		9
171	Hierarchical adaptive Multi-objective resource management for many-core systems. Journal of Systems Architecture, 2019, 97, 416-427.	4.3	9
172	The information processing factory. , 2019, , .		9
173	SEAMS. Transactions on Embedded Computing Systems, 2021, 20, 1-26.	2.9	9
174	Routing-Aware Application Mapping Considering Steiner Points for Coarse-Grained Reconfigurable Architecture. Lecture Notes in Computer Science, 2010, , 231-243.	1.3	9
175	Software controlled memory layout reorganization for irregular array access patterns. , 2007, , .		9
176	A comprehensive estimation technique for high-level synthesis. , 1995, , .		9
177	HCI and mHealth Wearable Tech: A Multidisciplinary Research Challenge. , 2020, , .		9
178	An Interpretable Machine Learning Model Enhanced Integrated CPU-GPU DVFS Governor. Transactions on Embedded Computing Systems, 2021, 20, 1-28.	2.9	9
179	A novel wireless ECG system for prolonged monitoring of multiple zebrafish for heart disease and drug screening studies. Biosensors and Bioelectronics, 2022, 197, 113808.	10.1	9
180	Memory-aware NoC Exploration and Design. , 2008, , .		8

#	Article	IF	Citations
181	AVid: Annotation driven video decoding for hybrid memories. , 2012, , .		8
182	HDGM: Hierarchical Dynamic Goal Management for Many-Core Resource Allocation. IEEE Embedded Systems Letters, 2018, 10, 61-64.	1.9	8
183	Design Methodology for Responsive and Rrobust MIMO Control of Heterogeneous Multicores. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 944-951.	2.4	8
184	Design methodologies for enabling self-awareness in autonomous systems. , 2018, , .		8
185	Optimal Application Mapping and Scheduling for Network-on-Chips with Computation in STT-RAM Based Router. IEEE Transactions on Computers, 2019, 68, 1174-1189.	3.4	8
186	Using Multimodal Assessments to Capture Personalized Contexts of College Student Well-being in 2020: Case Study. JMIR Formative Research, 2021, 5, e26186.	1.4	8
187	Memory size estimation for multimedia applications. , 1998, , .		8
188	Digital Healthâ€“Enabled Community-Centered Care: Scalable Model to Empower Future Community Health Workers Using Human-in-the-Loop Artificial Intelligence. JMIR Formative Research, 2022, 6, e29535.	1.4	8
189	Coordinated transformations for high-level synthesis of high performance microprocessor blocks. Proceedings - Design Automation Conference, 2002, , .	0.0	7
190	Access pattern-based memory and connectivity architecture exploration. Transactions on Embedded Computing Systems, 2003, 2, 33-73.	2.9	7
191	Towards practical high-level synthesis from large behavioral descriptions. , 2010, , .		7
192	Cross-Layer Exploration of Heterogeneous Multicore Processor Configurations. , 2015, , .		7
193	ViPZonE: Hardware Power Variability-Aware Virtual Memory Management for Energy Savings. IEEE Transactions on Computers, 2015, 64, 1483-1496.	3.4	7
194	Accuracy-Aware Power Management for Many-Core Systems Running Error-Resilient Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2749-2762.	3.1	7
195	SURF: Self-aware Unified Runtime Framework for Parallel Programs on Heterogeneous Mobile Architectures. , 2019, , .		7
196	Embodied Self-Aware Computing Systems. Proceedings of the IEEE, 2020, 108, 1027-1046.	21.3	7
197	The Causality Inference of Public Interest in Restaurants and Bars on Daily COVID-19 Cases in the United States: Google Trends Analysis. JMIR Public Health and Surveillance, 2021, 7, e22880.	2.6	7
198	Error-Exploiting Video Encoder to Extend Energy/QoS Tradeoffs for Mobile Embedded Systems. International Federation for Information Processing, 2008, , 23-34.	0.4	7

#	Article	IF	Citations
199	Combining Formal Verification with Observed System Execution Behavior to Tune System Parameters. Lecture Notes in Computer Science, 2007, , 257-273.	1.3	7
200	Encoding Techniques for On-Chip Communication Architectures. , 2008, , 253-300.		7
201	PoliMakE. , 2010, , .		7
202	Synthesis of Flexible Accelerators for Early Adoption of Ring-LWE Post-quantum Cryptography. Transactions on Embedded Computing Systems, 2020, 19, 1-17.	2.9	7
203	Methodology for multi-granularity embedded processor power model generation for an ESL design flow. , 2008, , .		7
204	V-SAT: A visual specification and analysis tool for system-on-chip exploration. Journal of Systems Architecture, 2001, 47, 263-275.	4.3	6
205	Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications. Design Automation for Embedded Systems, 2003, 8, 249-265.	1.0	6
206	Reducing code size for heterogeneous-connectivity-based VLIW DSPs through synthesis of instruction set extensions. , 2003, , .		6
207	A first look at the interplay of code reordering and configurable caches. , 2005, , .		6
208	Automated throughput-driven synthesis of bus-based communication architectures. , 2005, , .		6
209	Selective bandwidth and resource management in scheduling for dynamically reconfigurable architectures. Proceedings - Design Automation Conference, 2007, , .	0.0	6
210	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors. , 2008, , .		6
211	Cross-layer co-exploration of exploiting error resilience for video over wireless applications. , 2008, , .		6
212	Computing spike-based convolutions on GPUs. , 2009, , .		6
213	A Conservative Approximation Method for the Verification of Preemptive Scheduling Using Timed Automata. , 2009, , .		6
214	A novel NoC-based design for fault-tolerance of last-level caches in CMPs. , 2012, , .		6
215	Spiking neuron model of basal forebrain enhancement of visual attention. , 2012, , .		6
216	Variability-aware memory management for nanoscale computing. , 2013, , .		6

#	Article	IF	Citations
217	Thermal sensor allocation for SoCs based on temperature gradients. , 2015, , .		6
218	Protecting caches against multi-bit errors using embedded erasure coding. , 2015, , .		6
219	Automatic management of Software Programmable Memories in Manyâ€core Architectures. IET Computers and Digital Techniques, 2016, 10, 288-298.	1.2	6
220	SPMPool. Transactions on Embedded Computing Systems, 2016, 16, 1-27.	2.9	6
221	Small Memory Footprint Neural Network Accelerators. , 2019, , .		6
222	Flexible NTT Accelerators for RLWE Lattice-Based Cryptography. , 2019, , .		6
223	Dynamic iFogSim: A Framework for Full-Stack Simulation of Dynamic Resource Management in IoT Systems. , 2020, , .		6
224	Networks-On-Chip. , 2008, , 439-471.		6
225	Context-Aware Sensing via Dynamic Programming for Edge-Assisted Wearable Systems. ACM Transactions on Computing for Healthcare, 2020, 1, 1-25.	5.0	6
226	Optimal register assignment to loops for embedded code generation. , 1995, , .		6
227	Emergent Control of MPSoC Operation by a Hierarchical Supervisor / Reinforcement Learning Approach. , 2020, , .		6
228	Shift buffering technique for automatic code synthesis from synchronous dataflow graphs. , 2005, , .		5
229	Annotation Based Multimedia Streaming Over Wireless Networks. , 2006, , .		5
230	Incorporating PVT Variations in System-Level Power Exploration of On-Chip Communication Architectures. , 2008, , .		5
231	Constraint refinement for online verifiable cross-layer system adaptation. , 2008, , .		5
232	Evaluating memory architectures for media applications on Coarse-grained Reconfigurable Architectures. International Journal of Embedded Systems, 2008, 3, 119.	0.3	5
233	Electronic system-level design and high-level synthesis. , 2009, , 235-297.		5
234	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications. , 2009, , .		5

#	Article	IF	Citations
235	Dynamically reconfigurable on-chip communication architectures for multi use-case chip multiprocessor applications. , 2009, , .		5
236	Towards reverse engineering the brain: Modeling abstractions and simulation frameworks. , 2010, , .		5
237	ExCCel: Exploration of complementary cells for efficient DPA attack resistivity. , 2010, , .		5
238	Partitioning techniques for partially protected caches in resource-constrained embedded systems. ACM Transactions on Design Automation of Electronic Systems, 2010, 15, 1-30.	2.6	5
239	Slack-aware scheduling on Coarse Grained Reconfigurable Arrays. , 2011, , .		5
240	GPGPU accelerated simulation and parameter tuning for neuromorphic applications. , 2014, , .		5
241	Sense-making from Distributed and Mobile Sensing Data. , 2014, , .		5
242	Cooperative On-Chip Temperature EstimationUsing Multiple Virtual Sensors. IEEE Embedded Systems Letters, 2015, 7, 37-40.	1.9	5
243	Using a Flexible Fault-Tolerant Cache to Improve Reliability for Ultra Low Voltage Operation. Transactions on Embedded Computing Systems, 2015, 14, 1-24.	2.9	5
244	Dependability evaluation of SISO control-theoretic power managers for processor architectures. , 2017, , .		5
245	Goal Formulation: Abstracting Dynamic Objectives for Efficient On-chip Resource Allocation. , 2018, , .		5
246	Hierarchical dynamic goal management for IoT systems. , 2018, , .		5
247	ShaVe-ICE. Transactions on Embedded Computing Systems, 2018, 17, 1-25.	2.9	5
248	Self-Adaptive Memory Approximation: A Formal Control Theory Approach. IEEE Embedded Systems Letters, 2020, 12, 33-36.	1.9	5
249	SPECTR. ACM SIGPLAN Notices, 2018, 53, 169-183.	0.2	5
250	A hypergraph-based model for port allocation on multiple-register-file VLIW architectures. International Journal of Parallel Programming, 1995, 23, 499-513.	1.5	4
251	New directions in compiler technology for embedded systems (embedded tutorial). , 2001, , .		4
252	An Experimental Study on Energy Consumption of Video Encryption for Mobile Handheld Devices. , 0, , .		4

#	Article	IF	Citations
253	Floorplan driven leakage power aware IP-based SoC design space exploration. , 2006, , .		4
254	Constraint Refinement for Online Verifiable Cross-Layer System Adaptation. , 2008, , .		4
255	Cross-Abstraction Functional Verification and Performance Analysis of Chip Multiprocessor Designs. IEEE Transactions on Industrial Informatics, 2009, 5, 241-256.	11.3	4
256	DynaPoMP. , 2011, , .		4
257	Error-Aware Algorithm/Architecture Coexploration for Video Over Wireless Applications. Transactions on Embedded Computing Systems, 2012, 11S, 1-23.	2.9	4
258	SAM: Software-Assisted Memory Hierarchy for Scalable Manycore Embedded Systems. IEEE Embedded Systems Letters, 2017, 9, 109-112.	1.9	4
259	Quality-configurable memory hierarchy through approximation. , 2017, , .		4
260	MEMCOP: memory-aware co-operative power management governor for mobile games. Design Automation for Embedded Systems, 2018, 22, 95-116.	1.0	4
261	On the feasibility of SISO control-theoretic DVFS for power capping in CMPs. Microprocessors and Microsystems, 2018, 63, 249-258.	2.8	4
262	Classification of Electroencephalogram in a Mouse Model of Traumatic Brain Injury Using Machine Learning Approaches. , 2020, 2020, 3335-3338.		4
263	A Micro-Level Analysis of Physiological Responses to COVID-19: Continuous Monitoring of Pregnant Women in California. Frontiers in Public Health, 2022, 10, 808763.	2.7	4
264	AMSER: Adaptive Multimodal Sensing for Energy Efficient and Resilient eHealth Systems. , 2022, , .		4
265	High-level synthesis of scalable architectures for IIR filters using multichip modules. , 1993, , .		3
266	Partitioning of Variables for Multiple-Register-File VLIW Architectures. , 1994, , .		3
267	Efficient power reduction techniques for time multiplexed address buses. , 2002, , .		3
268	Proxy-based task partitioning of watermarking algorithms for reducing energy consumption in mobile devices. , 2004, , .		3
269	Video Stream Annotations for Energy Trade-offs in Multimedia Applications. , 2006, , .		3
270	Enabling heterogeneous cycle-based and event-driven simulation in a design flow integrated using the SPIRIT consortium specifications. Design Automation for Embedded Systems, 2007, 11, 119-140.	1.0	3

#	Article	IF	Citations
271	System-level PVT variation-aware power exploration of on-chip communication architectures. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-25.	2.6	3
272	Brain Derived Vision Algorithm on High Performance Architectures. International Journal of Parallel Programming, 2009, 37, 345-369.	1.5	3
273	On chip Communication-Architecture Based Thermal Management for SoCs. , 2009, , .		3
274	EAVE. Transactions on Embedded Computing Systems, 2012, 11, 1-28.	2.9	3
275	Minimal sparse observability of complex networks: Application to MPSoC sensor placement and run-time thermal estimation & tracking. , 2014, , .		3
276	Multicopy Cache. Transactions on Embedded Computing Systems, 2014, 13, 1-27.	2.9	3
277	The Case for Exploiting Underutilized Resources in Heterogeneous Mobile Architectures. , 2019, , .		3
278	Data Reuse for Accelerated Approximate Warps. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4623-4634.	2.7	3
279	A Technology-Based Pregnancy Health and Wellness Intervention (Two Happy Hearts): Case Study. JMIR Formative Research, 2021, 5, e30991.	1.4	3
280	Towards Smart and Efficient Health Monitoring Using Edge-enabled Situational-awareness. , 2021, , .		3
281	Architecture Description Languages. , 2007, , 59-76.		3
282	Self-aware Memory Management for Emerging Energy-efficient Architectures. , 2020, , .		3
283	On-Chip Dynamic Resource Managemen. Foundations and Trends in Electronic Design Automation, 2019, 13, 1-144.	1.0	3
284	Minimal sparse observability of complex networks: Application to MPSoC sensor placement and run-time thermal estimation & tracking. , 2014, , .		3
285	Functional verification of pipelined processors: a case study. , 0, , .		2
286	Energy efficient code generation exploiting reduced bit-width instruction set architectures (rISA). , 0, , .		2
287	Parlgran: parallelism granularity selection for scheduling task chains on dynamically reconfigurable architectures. , 0, , .		2
288	Tutorial 5: SoC Communication Architectures: Technology, Current Practice, Research, and Trends. , 2007, , .		2

#	Article	IF	Citations
289	Accelerating Brain Circuit Simulations of Object Recognition with CELL Processors. , 2007, , .		2
290	Managing leakage power and reliability in hot chips using system floorplanning and SRAM design. , 2008, , .		2
291	TRAM: A tool for Temperature and Reliability Aware Memory Design. , 2009, , .		2
292	Live demonstration: Computing spike-based convolutions on GPUs. , 2009, , .		2
293	Compiler-in-the-Loop Design Space Exploration Framework for Energy Reduction in Horizontally Partitioned Cache Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 461-465.	2.7	2
294	Neuromorphic modeling abstractions and simulation of large-scale cortical networks. , 2011, , .		2
295	Design space exploration and parameter tuning for neuromorphic applications. , 2013, , .		2
296	NoC-based fault-tolerant cache design in chip multiprocessors. Transactions on Embedded Computing Systems, 2014, 13, 1-26.	2.9	2
297	Orchestrated application quality and energy storage management in solar-powered embedded systems. , 2015, , .		2
298	On Detecting and Using Memory Phases in Multimedia Systems. , 2016, , .		2
299	Guest Editorial: Special Issue on Self-Aware Systems on Chip. IEEE Design and Test, 2017, 34, 6-7.	1.2	2
300	Trends in On-chip Dynamic Resource Management. , 2018, , .		2
301	DNN-Assisted Sensor for Energy-Efficient ECG Monitoring. , 2019, , .		2
302	Intelligent Management of Mobile Systems Through Computational Self-Awareness. Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series, 2021, , 41-73.	0.5	2
303	Data Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures. International Federation for Information Processing, 2008, , 213-225.	0.4	2
304	On-Chip Communication Architecture Standards. , 2008, , 43-100.		2
305	Reclocking for high-level synthesis. , 1995, , .		2
306	Data Reuse Driven Memory and Network-On-Chip Co-Synthesis. , 2007, , 299-312.		2

#	Article	IF	Citations
307	Hybrid Learning for Orchestrating Deep Learning Inference in Multi-user Edge-cloud Networks. , 2022, , .		2
308	Design reuse (panel). , 1994, , .		1
309	Energy-Aware Adaptations for End-to-End Videostreaming to Mobile Handheld Devices. , 2004, , 255-273.		1
310	FIFO power optimization for on-chip networks. , 2004, , .		1
311	A methodology for validation of microprocessors using symbolic simulation. International Journal of Embedded Systems, 2005, 1, 14.	0.3	1
312	Probability Based Power Aware Error Resilient Coding. , 0, , .		1
313	Functional and Timing Validation of Partially Bypassed Processor Pipelines. , 2007, , .		1
314	A Compiler-in-the-Loop framework to explore Horizontally Partitioned Cache architectures. , 2008, , .		1
315	Cross-Layer Approaches to Designing Reliable Systems Using Unreliable Chips. , 2008, , .		1
316	ESL hand-off. , 2008, , .		1
317	Introduction to Architecture Description Languages. , 2008, , 1-12.		1
318	Adaptive reduced bit-width Instruction Set Architecture (adapt-rISA). , 2009, , .		1
319	Combining code reordering and cache configuration. Transactions on Embedded Computing Systems, 2012, 11, 1-20.	2.9	1
320	Modeling and Analysis of Fault-tolerant Distributed Memories for Networks-on-Chip. , 2013, , .		1
321	An advanced course design for mobile embedded software through Android programming. , 2013, , .		1
322	A Reliable, Safe, and Secure Run-Time Platform for Cyber Physical Systems. , 2013, , .		1
323	Cross-layer virtual/physical sensing and actuation for resilient heterogeneous many-core SoCs. , 2016, , .		1
324	Exploring fast and slow memories in HMP core types. , 2017, , .		1

#	Article	IF	Citations
325	PoliCym. , 2017, , .		1
326	Guest Editorial: Special Issue on Self-Aware Systems on Chip. IEEE Design and Test, 2018, 35, 5-6.	1.2	1
327	Exploring Hybrid Memory Caches in Chip Multiprocessors. , 2018, , .		1
328	Aggressive Memory-Aware Compilation. Lecture Notes in Computer Science, 2001, , 147-151.	1.3	1
329	Compiler driven data layout optimization for regular/irregular array access patterns. ACM SIGPLAN Notices, 2008, 43, 41-50.	0.2	1
330	Basic Concepts of Bus-Based Communication Architectures. , 2008, , 17-41.		1
331	Emerging On-Chip Interconnect Technologies. , 2008, , 473-507.		1
332	Introduction to the Special Issue on Self-Aware Cyber-physical Systems. ACM Transactions on Cyber-Physical Systems, 2020, 4, 1-2.	2.5	1
333	Reflecting on Self-Aware Systems-on-Chip. , 2021, , 79-95.		1
334	Investigation of Machine Learning and Deep Learning Approaches for Detection of Mild Traumatic Brain Injury from Human Sleep Electroencephalogram. , 2021, 2021, 6134-6137.		1
335	An Introduction to the Plasma Language. International Workshop on Microprocessor Test and Verification, 2005, , .	0.0	0
336	Minimizing peak power for application chains on architectures with partial dynamic reconfiguration. , 2006, , .		0
337	Memory optimal single appearance schedule with dynamic loop count for synchronous dataflow graphs. , 0, , .		0
338	Annotation Integration and Trade-off Analysis for Multimedia Applications. , 2007, , .		0
339	Using FORAY Models to Enable MPSoC Memory Optimizations. International Journal of Parallel Programming, 2008, 36, 93-113.	1.5	0
340	Quo vadis, BTSoC (Billion Transistor SoC)?. , 2008, , .		0
341	Real-time analysis of resource-constrained distributed systems by simulation-guided model checking. ACM SIGBED Review, 2008, 5, 1-2.	1.8	0
342	CODES+ISSS 2007 guest editorsâ€™ introduction. Design Automation for Embedded Systems, 2009, 13, 51-52.	1.0	0

#	Article	IF	Citations
343	QoS-aware dynamic power management for coarse-grained reconfigurable architecture. , 2009, , .		0
344	Multiple sleep modes leakage control in peripheral circuits of a all major SRAM-based processor units. , 2010, , .		0
345	Bandwidth Management in Application Mapping for Dynamically Reconfigurable Architectures. ACM Transactions on Reconfigurable Technology and Systems, 2010, 3, 1-30.	2.5	0
346	Keynote speach. , 2012, , .		0
347	Guest Editorial Special Section on Memory Architectures and Organization. IEEE Embedded Systems Letters, 2012, 4, 81-81.	1.9	0
348	Outlook for many-core systems: Cloudy with a chance of virtualization. , 2013, , .		0
349	Vision-inspired global routing for enhanced performance and reliability. , 2013, , .		0
350	Characterization of GPGPU Workloads via Correlation-Driven Kernel Similarity Analysis. , 2013, , .		0
351	Heat-aware transmission strategies. , 2015, , .		0
352	HAMEX. , 2016, , .		0
353	Empowering autonomy through self-awareness in MPSoCs. , 2017, , .		0
354	Exploring Heterogeneous Task-Level Parallelism in a BMA Video Coding Application using System-Level Simulation. , 2018, , .		0
355	Self-Awareness for Heterogeneous MPSoCs. , 2018, , .		0
356	The power impact of hardware and software actuators on self-adaptable many-core systems. Journal of Systems Architecture, 2019, 97, 42-53.	4.3	0
357	Predicting Failures in Embedded Systems Using Long Short-Term Inference. IEEE Embedded Systems Letters, 2021, 13, 85-89.	1.9	0
358	Exploring Energy Efficient Architectures for RLWE Lattice-Based Cryptography. Journal of Signal Processing Systems, 0, , 1.	2.1	0
359	Data Collection and Labeling of Real-Time IoT-Enabled Bio-Signals in Everyday Settings for Mental Health Improvement. , 2021, , .		0
360	Customizing Software Toolkits for Embedded Systems-on-Chip. IFIP Advances in Information and Communication Technology, 2001, , 87-97.	0.7	0

#	Article	IF	Citations
361	Compiler-Aided Design of Embedded Computers. , 2007, , 3-1-3-36.		0
362	Models for Power and Thermal Estimation. , 2008, , 143-184.		0
363	Models for Performance Exploration. , 2008, , 101-142.		0
364	Verification and Security Issues in On-Chip Communication Architecture Design. , 2008, , 367-402.		0
365	EXPRESSION. , 2008, , 133-161.		0
366	A Formal Methodology for Compositional Cross-Layer Optimization. Lecture Notes in Computer Science, 2011, , 207-222.	1.3	0
367	Copy Elimination for Parallelizing Compilers. Lecture Notes in Computer Science, 1999, , 275-289.	1.3	0
368	Microarchitecture-Level SoC Design. , 2016, , 1-46.		0
369	Architecture and Cross-Layer Design Space Exploration. , 2016, , 1-24.		0
370	Robust Face Recognition Against Soft-errors Using a Cross-layer Approach. International Journal of Computers, Communications and Control, 2016, 11, 657.	1.8	0
371	Architecture and Cross-Layer Design Space Exploration. , 2017, , 247-270.		0
372	Microarchitecture-Level SoC Design. , 2017, , 867-913.		0
373	Effect of Soft Errors in Iterative Learning Control and Compensation using Cross-layer Approach. International Journal of Computers, Communications and Control, 2019, 14, 359-374.	1.8	0
374	Exploiting Memory Resilience for Emerging Technologies: An Energy-Aware Resilience Exemplar for STT-RAM Memories. Embedded Systems, 2021, , 505-526.	0.6	0
375	Exploiting Heterogeneous Mobile Architectures Through a Unified Runtime Framework. IFIP Advances in Information and Communication Technology, 2020, , 323-344.	0.7	0
376	Modeling of Software-Hardware Complexes. , 2007, , 423-425.		0