Bipin Rajendran

List of Publications by Year
in descending order

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68	5,053	304743	377865
papers	citations	22 h-index	34 g-index

68	68	68	4793
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Hybrid In-Memory Computing Architecture for the Training of Deep Neural Networks. , 2021, , .		0
2	Training multi-layer spiking neural networks using NormAD based spatio-temporal error backpropagation. Neurocomputing, 2020, 380, 67-77.	5.9	15
3	An On-Chip Learning Accelerator for Spiking Neural Networks using STT-RAM Crossbar Arrays. , 2020, , .		3
4	Memristorsâ€"From Inâ€Memory Computing, Deep Learning Acceleration, and Spiking Neural Networks to the Future of Neuromorphic and Bioâ€Inspired Computing. Advanced Intelligent Systems, 2020, 2, 2000085.	6.1	143
5	Accurate deep neural network inference using computational phase-change memory. Nature Communications, 2020, 11, 2473.	12.8	263
6	Mixed-Precision Deep Learning Based on Computational Memory. Frontiers in Neuroscience, 2020, 14, 406.	2.8	61
7	Experimental Demonstration of Supervised Learning in Spiking Neural Networks with Phase-Change Memory Synapses. Scientific Reports, 2020, 10, 8080.	3.3	48
8	Bio-mimetic synaptic plasticity and learning in a sub-500ÂmV Cu/SiO2/W memristor. Microelectronic Engineering, 2020, 226, 111290.	2.4	11
9	Role of resistive memory devices in brain-inspired computing. , 2020, , 3-16.		7
10	Memristive devices for spiking neural networks. , 2020, , 399-405.		1
11	Memristive devices as computational memory. , 2020, , 167-174.		0
12	Building Next-Generation AI systems: Co-Optimization of Algorithms, Architectures, and Nanoscale Memristive Devices. , 2019, , .		1
13	Low-Power Neuromorphic Hardware for Signal Processing Applications: A Review of Architectural and System-Level Design Approaches. IEEE Signal Processing Magazine, 2019, 36, 97-110.	5.6	88
14	Neuromorphic Hardware Accelerator for SNN Inference based on STT-RAM Crossbar Arrays. , 2019, , .		9
15	Learning First-to-Spike Policies for Neuromorphic Control Using Policy Gradients. , 2019, , .		6
16	Spiking neural networks for handwritten digit recognitionâ€"Supervised learning and network optimization. Neural Networks, 2018, 103, 118-127.	5.9	100
17	Well-Posed Verilog-A Compact Model for Phase Change Memory. , 2018, , .		2
18	Stochastic learning in deep neural networks based on nanoscale PCMO device characteristics. Neurocomputing, 2018, 321, 227-236.	5.9	12

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19	A phase-change memory model for neuromorphic computing. Journal of Applied Physics, 2018, 124, .	2.5	96
20	Live Demonstration: Image Classification Using Bio-inspired Spiking Neural Networks. , 2018, , .		0
21	Neuromorphic computing with multi-memristive synapses. Nature Communications, 2018, 9, 2514.	12.8	566
22	Acceleration of Convolutional Networks Using Nanoscale Memristive Devices. Communications in Computer and Information Science, 2018, , 240-251.	0.5	1
23	Building Brain-Inspired Computing Systems: Examining the Role of Nanoscale Devices. IEEE Nanotechnology Magazine, 2018, 12, 19-35.	1.3	30
24	Modeling and Simulation of 1/f Noise During Threshold Switching for Phase Change Memory. Lecture Notes in Electrical Engineering, 2018, , 77-83.	0.4	1
25	Arbitrary Spike Time Dependent Plasticity (STDP) in Memristor by Analog Waveform Engineering. IEEE Electron Device Letters, 2017, 38, 740-743.	3.9	57
26	Spiking neural networks â€" Algorithms, hardware implementations and applications. , 2017, , .		9
27	Learning and real-time classification of hand-written digits with spiking neural networks. , 2017, , .		5
28	Stochastic deep learning in memristive networks. , 2017, , .		2
29	Novel Biomimetic Si Devices for Neuromorphic Computing Architecture. Cognitive Systems Monographs, 2017, , 151-174.	0.1	0
30	Physics-based switching model for Cu/SiO<inf>2</inf>/W quantum memristor. , 2016, , .		1
31	Verilog-A compact model for a novel Cu/SiO<inf>2</inf>/W quantum memristor. , 2016, , .		2
32	A 250 mV Cu/SiO₂/W Memristor with Half-Integer Quantum Conductance States. Nano Letters, 2016, 16, 1602-1608.	9.1	92
33	Neuromorphic Computing Based on Emerging Memory Technologies. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 198-211.	3.6	96
34	C. elegans chemotaxis inspired neuromorphic circuit for contour tracking and obstacle avoidance. , 2015, , .		10
35	Delayed Guidance: A Teaching-Learning Strategy to Develop Ill-Structured Problem Solving Skills in Engineering. , 2015, , .		3
36	A circuit model for a Si-based biomimetic synaptic time-keeping device. , 2015, , .		1

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37	Composer classification based on temporal coding in adaptive spiking neural networks. , 2015, , .		1
38	Live demonstration: Spiking neural circuit based navigation inspired by C. elegans thermotaxis. , 2015, , .		1
39	Increasing reconfigurability with memristive interconnects. , 2015, , .		2
40	Reducing read latency of phase change memory via early read and Turbo Read. , 2015, , .		26
41	NormAD - Normalized Approximate Descent based supervised learning rule for spiking neurons. , 2015, , .		33
42	Arithmetic computing via rate coding in neural circuits with spike-triggered adaptive synapses. , 2015, , .		0
43	Programming Current Reduction via Enhanced Asymmetry-Induced Thermoelectric Effects in Vertical Nanopillar Phase-Change Memory Cells. IEEE Transactions on Electron Devices, 2015, 62, 4015-4021.	3.0	7
44	Scalable Digital CMOS Architecture for Spike Based Supervised Learning. Communications in Computer and Information Science, 2015, , 149-158.	0.5	2
45	Analog memristive time dependent learning using discrete nanoscale RRAM devices. , 2014, , .		8
46	Guided Problem Solving and Group Programming: A Technology-Enhanced Teaching-Learning Strategy for Engineering Problem Solving. , 2014, , .		3
47	Mimicking the worm — An adaptive spiking neural circuit for contour tracking inspired by C. Elegans thermotaxis. , 2014, , .		8
48	Novel synaptic memory device for neuromorphic computing. Scientific Reports, 2014, 4, 5333.	3.3	85
49	Nanoscale electronic synapses using phase change devices. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-20.	2.3	123
50	On Pairing of Bipolar RRAM Memory With NPN Selector Based on Set/Reset Array Power Considerations. IEEE Nanotechnology Magazine, 2013, 12, 1178-1184.	2.0	11
51	Embedded tutorial - Can silicon machines match the efficiency of the human brain?. , 2013, , .		1
52	Specifications of Nanoscale Devices and Circuits for Neuromorphic Computational Systems. IEEE Transactions on Electron Devices, 2013, 60, 246-253.	3.0	139
53	Pulsed laser annealing: A scalable and practical technology for monolithic 3D IC. , 2013, , .		9
54	Integrated on-chip inductors with electroplated magnetic yokes (invited). Journal of Applied Physics, 2012, 111, .	2.5	43

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55	Efficient scrub mechanisms for error-prone emerging memories. , 2012, , .		101
56	A 45nm CMOS neuromorphic chip with a scalable architecture for learning in networks of spiking neurons. , 2011, , .		190
57	Driving Device Comparison for Phase-Change Memory. IEEE Transactions on Electron Devices, 2011, 58, 664-671.	3.0	8
58	Demonstration of CAM and TCAM Using Phase Change Devices. , 2011, , .		23
59	Phase Change Memory: From Devices to Systems. Synthesis Lectures on Computer Architecture, 2011, 6, 1-134.	1.3	52
60	Phase Change Memory. Proceedings of the IEEE, 2010, 98, 2201-2227.	21.3	1,420
61	Phase change memory technology. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2010, 28, 223-262.	1.2	795
62	Dynamic Resistance—A Metric for Variability Characterization of Phase-Change Memory. IEEE Electron Device Letters, 2009, 30, 126-129.	3.9	22
63	Optimized Scaling of Diode Array Design for 32nm Node Phase Change Memory. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	3
64	Phase change memory â€" opportunities and challenges. , 2007, , .		4
65	Nano-graphoepitaxy of semiconductors for 3D integration. Microelectronic Engineering, 2007, 84, 891-894.	2.4	10
66	Lamellar crystallization of silicon for 3-dimensional integration. Microelectronic Engineering, 2007, 84, 1186-1189.	2.4	8
67	Low Thermal Budget Processing for Sequential 3-D IC Fabrication. IEEE Transactions on Electron Devices, 2007, 54, 707-714.	3.0	56
68	Silicon nanowires for sequence-specific DNA sensing: device fabrication and simulation. Applied Physics A: Materials Science and Processing, 2005, 80, 1257-1263.	2.3	117