

Massoud Pedram

List of Publications by Year in descending order

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514
papers

10,947
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87723

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all docs

519
docs citations

519
times ranked

6269
citing authors

#	ARTICLE	IF	CITATIONS
1	An Adaptive Memory-Side Encryption Method for Improving Security and Lifetime of PCM-Based Main Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1744-1756.	1.9	3
2	High-Radix Design of a Scalable Montgomery Modular Multiplier With Low Latency. IEEE Transactions on Computers, 2022, 71, 436-449.	2.4	5
3	A ² P-MANN: Adaptive Attention Inference Hops Pruned Memory-Augmented Neural Networks. IEEE Transactions on Neural Networks and Learning Systems, 2022, PP, 1-13.	7.2	0
4	All-Digital Phase-Locked Loop in Single Flux Quantum Circuit Technology. IEEE Transactions on Applied Superconductivity, 2022, 32, 1-8.	1.1	1
5	Posit Process Element for Using in Energy-Efficient DNN Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 844-848.	2.1	2
6	HiPerRF: A Dual-Bit Dense Storage SFQ Register File. , 2022, , .		3
7	DigiQ: A Scalable Digital Controller for Quantum Computers Using SFQ Logic. , 2022, , .		10
8	BMPQ: Bit-Gradient Sensitivity-Driven Mixed-Precision Quantization of DNNs from Scratch. , 2022, , .		6
9	X-NVDLA: Runtime Accuracy Configurable NVDLA based on Employing Voltage Overscaling Approach. , 2022, , .		1
10	An Efficient Error Estimation Technique for Pruning Approximate Data-Flow Graphs in Design Space Exploration. , 2022, , .		1
11	Sparse Periodic Systolic Dataflow for Lowering Latency and Power Dissipation of Convolutional Neural Network Accelerators. , 2022, , .		0
12	Developing TEI-Aware Ultralow-Power SoC Platforms for IoT End Nodes. IEEE Internet of Things Journal, 2021, 8, 4642-4656.	5.5	10
13	JointDNN: An Efficient Training and Inference Engine for Intelligent Mobile Cloud Computing Services. IEEE Transactions on Mobile Computing, 2021, 20, 565-576.	3.9	145
14	Therminator 2: A Fast Thermal Simulator for Portable Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2528-2541.	1.9	7
15	Depth-bounded Graph Partitioning Algorithm and Dual Clocking Method for Realization of Superconducting SFQ Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-22.	1.8	2
16	OPTIMA: An Approach for Online Management of Cache Approximation Levels in Approximate Processing Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 434-446.	2.1	0
17	Coarse2Fine: a two-stage training method for fine-grained visual classification. Machine Vision and Applications, 2021, 32, 1.	1.7	6
18	NullaNet Tiny: Ultra-low-latency DNN Inference Through Fixed-function Combinational Logic. , 2021, , .		6

#	ARTICLE	IF	CITATIONS
19	qMC. , 2021, , .		4
20	Loading-Aware Reliability Improvement of Ultra-Low Power Memristive Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3411-3421.	3.5	3
21	A Variation-aware Hold Time Fixing Methodology for Single Flux Quantum Logic Circuits. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-17.	1.9	0
22	An 8-b Multiplier Using Single-Stage Full Adder Cell in Single-Flux-Quantum Circuit Technology. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-10.	1.1	7
23	CD-DFT: A Current-Difference Design-for-Testability to Detect Short Defects of STT-MRAM Under Process Variations. IEEE Transactions on Device and Materials Reliability, 2021, 21, 436-443.	1.5	4
24	LATIM: Loading-Aware Offline Training Method for Inverter-Based Memristive Neural Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3346-3350.	2.2	5
25	Reliability Enhancement of Inverter-Based Memristor Crossbar Neural Networks Using Mathematical Analysis of Circuit Non-Idealities. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4310-4323.	3.5	8
26	DNR. , 2021, , .		18
27	Spike-Thrift: Towards Energy-Efficient Deep Spiking Neural Networks by Limiting Spiking Activity via Attention-Guided Compression. , 2021, , .		37
28	A Logic Verification Framework for SFQ and AQFP Superconducting Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-11.	1.1	3
29	qSeq: Full Algorithmic and Tool Support for Synthesizing Sequential Circuits in Superconducting SFQ Technology. , 2021, , .		2
30	HIRE-SNN: Harnessing the Inherent Robustness of Energy-Efficient Deep Spiking Neural Networks by Training with Crafted Input Noise. , 2021, , .		21
31	Block-Based Carry Speculative Approximate Adder for Energy-Efficient Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 137-141.	2.2	43
32	DART: A Framework for Determining Approximation Levels in an Approximable Memory Hierarchy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 273-286.	2.1	7
33	X-CGRA: An Energy-Efficient Approximate Coarse-Grained Reconfigurable Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2558-2571.	1.9	31
34	RandShift: An Energy-Efficient Fault-Tolerant Method in Secure Nonvolatile Main Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 287-291.	2.1	4
35	An Efficient Pipelined Architecture for Superconducting Single Flux Quantum Logic Circuits Utilizing Dual Clocks. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-12.	1.1	17
36	SystemVerilog Modeling of SFQ and AQFP Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-13.	1.1	12

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37	Res-DNN: A Residue Number System-Based DNN Accelerator Unit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 658-671.	3.5	37
38	POLAR: A Pipelined/Overlapped FPGA-Based LSTM Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 838-842.	2.1	32
39	Energy Efficiency in 5G Cellular Network Systems. IEEE Design and Test, 2020, 37, 64-78.	1.1	4
40	Circuit-Level Techniques for Logic and Memory Blocks in Approximate Computing Systemsx. Proceedings of the IEEE, 2020, 108, 2150-2177.	16.4	16
41	Static Timing Analysis (STA) with Timing Bleed: Certifying Much Higher Performance for Rapid Single Flux Quantum (RSFQ) Logic. Journal of Physics: Conference Series, 2020, 1559, 012003.	0.3	3
42	EGAN: A Framework for Exploring the Accuracy vs. Energy Efficiency Trade-off in Hardware Implementation of Error Resilient Applications. , 2020, , .		5
43	A Stochastic Framework for Virtualization Layer Deployment in Vehicular Cloud Networks. , 2020, , .		1
44	NN-PARS: A Parallelized Neural Network Based Circuit Simulation Framework. , 2020, , .		1
45	qSTA: A Statistical Static Timing Analysis Tool for Superconducting Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-12.	1.1	7
46	A Timing Uncertainty-Aware Clock Tree Topology Generation Algorithm for Single Flux Quantum Circuits. , 2020, , .		4
47	NISQ+: Boosting quantum computing power by approximating quantum error correction. , 2020, , .		34
48	Q ² -DNN: A Hybrid DSP-LUT-Based Processing Unit With Operation Packing and Out-of-Order Execution for Efficient Realization of Convolutional Neural Networks on FPGA Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3056-3069.	3.5	2
49	Offline Training Improvement of Inverter-Based Memristive Neural Networks Using Inverter Voltage Characteristic Smoothing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3442-3446.	2.2	4
50	Pre-defined Sparsity for Low-Complexity Convolutional Neural Networks. IEEE Transactions on Computers, 2020, , 1-1.	2.4	29
51	qSTA: A Static Timing Analysis Tool for Superconducting Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-9.	1.1	6
52	Design Exploration of Energy-Efficient Accuracy-Configurable Dadda Multipliers With Improved Lifetime Based on Voltage Overscaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1207-1220.	2.1	24
53	Postrouting Optimization of the Working Clock Frequency of Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-14.	1.1	1
54	Deep-PowerX. , 2020, , .		5

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55	Interstice: Inverter-Based Memristive Neural Networks Discretization for Function Approximation Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1578-1588.	2.1	9
56	TDP-ADMM: A Timing Driven Placement Approach for Superconductive Electronic Circuits Using Alternating Direction Method of Multipliers. , 2020, , .		4
57	Retiming for high-performance superconductive circuits with register energy minimization. , 2020, , .		1
58	Runtime Deep Model Multiplexing for Reduced Latency and Energy Consumption Inference. , 2020, , .		4
59	ACHILLES: Accuracy-Aware High-Level Synthesis Considering Online Quality Management. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1452-1465.	1.9	3
60	TEI-UQP: Exploiting Body Biasing to Improve the TEI-Aware Ultralow Power Methods. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1758-1770.	1.9	7
61	A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 327-340.	3.5	30
62	Approximate Logic Synthesis: A Reinforcement Learning-Based Technology Mapping Approach. , 2019, , .		13
63	VeriSFQ: A Semi-formal Verification Framework and Benchmark for Single Flux Quantum Technology. , 2019, , .		16
64	qGDR: A Via-Minimization-Oriented Routing Tool for Large-Scale Superconductive Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-12.	1.1	16
65	TIP: A Temperature Effect Inversion-Aware Ultra-Low Power System-on-Chip Platform. , 2019, , .		7
66	OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4687-4698.	3.5	12
67	Towards Green Mobile Networks: Concurrent User Association and Dynamic Switching in Cells. , 2019, , .		1
68	A Meta-Learning Approach for Custom Model Training. Proceedings of the AAAI Conference on Artificial Intelligence, 2019, 33, 9937-9938.	3.6	1
69	A Minimum-Skew Clock Tree Synthesis Algorithm for Single Flux Quantum Logic Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-13.	1.1	20
70	Towards Collaborative Intelligence Friendly Architectures for Deep Learning. , 2019, , .		19
71	BottleNet: A Deep Learning Architecture for Intelligent Mobile Cloud Computing Services. , 2019, , .		89
72	Deep Learning-Based Circuit Recognition Using Sparse Mapping and Level-Dependent Decaying Sum Circuit Representations. , 2019, , .		16

#	ARTICLE	IF	CITATIONS
73	CSrram: Area-Efficient Low-Power Ex-Situ Training Framework for Memristive Neuromorphic Circuits Based on Clustered Sparsity. , 2019, , .		5
74	Timing Characterization for Static Timing Analysis of Single Flux Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-8.	1.1	13
75	TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1161-1173.	2.1	93
76	ColdFlux Superconducting EDA and TCAD Tools Project: Overview and Progress. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-7.	1.1	50
77	Energy-efficient, low-latency realization of neural networks through boolean logic minimization. , 2019, , .		26
78	Hybrid Cell Assignment and Sizing for Power, Area, Delay-Product Optimization of SRAM Arrays. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 2047-2051.	2.2	3
79	A Hybrid Framework for Functional Verification using Reinforcement Learning and Deep Learning. , 2019, , .		3
80	Balanced Factorization and Rewriting Algorithms for Synthesizing Single Flux Quantum Logic Circuits. , 2019, , .		8
81	Simulation Analysis and Energy-Saving Techniques for ERSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-7.	1.1	14
82	kNN-CAM: A k-Nearest Neighbors-based Configurable Approximate Floating Point Multiplier. , 2019, , .		8
83	Design Space Exploration of Memory Controller Placement in Throughput Processors with Deep Learning. IEEE Computer Architecture Letters, 2019, 18, 51-54.	1.0	7
84	qCG: A Low-Power Multi-Domain SFQ Logic Design and Verification Framework. , 2019, , .		4
85	A Statistical Static Timing Analysis Tool for Superconducting Single-Flux-Quantum Circuits. , 2019, , .		5
86	A Dynamic Programming-Based, Path Balancing Technology Mapping Algorithm Targeting Area Minimization. , 2019, , .		14
87	CSM-NN: Current Source Model Based Logic Circuit Simulation - A Neural Network Approach. , 2019, , .		4
88	A Clock Synthesis Algorithm for Hierarchical Chains of Homogeneous Clover-Leaves Clock Networks for Single Flux Quantum Logic Circuits. , 2019, , .		0
89	Design of an SFQ Full Adder as a Single-Stage Gate. , 2019, , .		2
90	A Hyper-Parameter Based Margin Calculation Algorithm for Single Flux Quantum Logic Cells. , 2019, , .		2

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91	Low-power data encoding/decoding for energy-efficient static random access memory design. IET Circuits, Devices and Systems, 2019, 13, 1152-1159.	0.9	5
92	PBMap: A Path Balancing Technology Mapping Algorithm for Single Flux Quantum Logic Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-14.	1.1	38
93	Hierarchical, Portfolio Theory-Based Virtual Machine Consolidation in a Compute Cloud. IEEE Transactions on Services Computing, 2018, 11, 63-77.	3.2	13
94	An Efficient False Path-Aware Heuristic Critical Path Selection Method with High Coverage of the Process Variation Space. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-25.	1.9	2
95	PHAX: Physical Characteristics Aware <italic>Ex-Situ</italic> Training Framework for Inverter-Based Memristive Neuromorphic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1602-1613.	1.9	20
96	An Ultra Low-Power Memristive Neuromorphic Circuit for Internet of Things Smart Sensors. IEEE Internet of Things Journal, 2018, 5, 1011-1022.	5.5	32
97	Superconducting Magnetic Field Programmable Gate Array. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-12.	1.1	25
98	Lifetime improvement by exploiting aggressive voltage scaling during runtime of error-resilient applications. The Integration VLSI Journal, 2018, 61, 29-38.	1.3	14
99	Accurate margin calculation for single flux quantum logic cells. , 2018, , .		7
100	TheSPoT: Thermal Stress-Aware Power and Temperature Management for Multiprocessor Systems-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1532-1545.	1.9	26
101	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1089-1093.	2.2	98
102	An Exploration of Applying Gate-Length-Biasing Techniques to Deeply-Scaled FinFETs Operating in Multiple Voltage Regimes. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 172-183.	3.2	7
103	TEI-NoC: Optimizing Ultralow Power NoCs Exploiting the Temperature Effect Inversion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 458-471.	1.9	16
104	Design automation methodology and tools for superconductive electronics. , 2018, , .		10
105	Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2530-2541.	2.1	58
106	Energy-Efficient Computing: Datacenters, Mobile Devices, and Mobile Clouds. , 2018, , .		0
107	Power Management of Cache-Enabled Cooperative Base Stations Towards Zero Grid Energy. , 2018, , .		5
108	Toward Approximate Computing for Coarse-Grained Reconfigurable Architectures. IEEE Micro, 2018, 38, 63-72.	1.8	16

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109	SFQmap: A Technology Mapping Tool for Single Flux Quantum Logic Circuits. , 2018, , .		27
110	Opportunities for Machine Learning in Electronic Design Automation. , 2018, , .		20
111	A 125mV 2ns-access-time 16Kb SRAM design based on a 6T hybrid TFET-FinFET cell. , 2018, , .		1
112	An Energy-Efficient, Yet Highly-Accurate, Approximate Non-Iterative Divider. , 2018, , .		11
113	Energy and Performance Efficient Computation Offloading for Deep Neural Networks in a Mobile Cloud Computing Environment. , 2018, , .		60
114	Logic Optimization, Complex Cell Design, and Retiming of Single Flux Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2018, 28, 1-9.	1.1	25
115	Energy and Reliability Improvement of Voltage-Based, Clustered, Coarse-Grain Reconfigurable Architectures by Employing Quality-Aware Mapping. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 480-493.	2.7	17
116	A hardware-friendly algorithm for scalable training and deployment of dimensionality reduction models on FPGA. , 2018, , .		8
117	A placement algorithm for superconducting logic circuits based on cell grouping and super-cell placement. , 2018, , .		14
118	FFT-based deep learning deployment in embedded systems. , 2018, , .		29
119	Internal writeâ€back and readâ€beforeâ€write schemes to eliminate the disturbance to the halfâ€selected cells in SRAMs. IET Circuits, Devices and Systems, 2018, 12, 460-466.	0.9	20
120	VIBNN. , 2018, , .		39
121	PX-CGRA: Polymorphic approximate coarse-grained reconfigurable architecture. , 2018, , .		29
122	Energy Consumption and Lifetime Improvement of Coarse-Grained Reconfigurable Architectures Targeting Low-Power Error-Tolerant Applications. , 2018, , .		5
123	Toward Enabling Automated Cognition and Decision-Making in Complex Cyber-Physical Systems. , 2018, , .		8
124	VIBNN. ACM SIGPLAN Notices, 2018, 53, 476-488.	0.2	32
125	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1352-1361.	2.1	188
126	Design of multiple fanout clock distribution network for rapid single flux quantum technology. , 2017, , .		17

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127	An energy and area efficient yet high-speed square-root carry select adder structure. Computers and Electrical Engineering, 2017, 58, 101-112.	3.0	9
128	CALM. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-21.	1.9	1
129	An Integrated Row-Based Cell Placement and Interconnect Synthesis Tool for Large SFQ Logic Circuits. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-8.	1.1	61
130	Pilot Register File: Energy Efficient Partitioned Register File for GPUs. , 2017, , .		26
131	Optimal Joint Management of Charging and Battery Swapping Services for Electric Vehicles. , 2017, , .		3
132	TruncApp: A truncation-based approximate divider for energy efficient DSP applications. , 2017, , .		33
133	TEI-power. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-25.	1.9	8
134	Robust neuromorphic computing in the presence of process variation. , 2017, , .		12
135	Efficient Critical Path Identification Based on Viability Analysis Method Considering Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2668-2672.	2.1	4
136	A thermally-aware energy minimization methodology for global interconnects. , 2017, , .		0
137	High-performance FPGA implementation of equivariant adaptive separation via independence algorithm for Independent Component Analysis. , 2017, , .		4
138	Optimal Control of PEVs with a Charging Aggregator Considering Regulation Service Provisioning. ACM Transactions on Cyber-Physical Systems, 2017, 1, 1-23.	1.9	1
139	Robust Hybrid TFET-MOSFET Circuits in Presence of Process Variations and Soft Errors. IFIP Advances in Information and Communication Technology, 2017, , 41-59.	0.5	0
140	LETAM: A low energy truncation-based approximate multiplier. Computers and Electrical Engineering, 2017, 63, 1-17.	3.0	34
141	Hybrid TFET-MOSFET circuit: A solution to design soft-error resilient ultra-low power digital circuit. The Integration VLSI Journal, 2017, 57, 11-19.	1.3	9
142	An optimal energy co-scheduling framework for smart buildings. The Integration VLSI Journal, 2017, 58, 528-537.	1.3	11
143	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 393-401.	2.1	130
144	Gate-all-around FET based 6T SRAM design using a device-circuit co-optimization framework. , 2017, , .		3

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145	Context-driven power management in cache-enabled base stations using a Bayesian neural network. , 2017, , .		5
146	Design of Complex Rapid Single-Flux-Quantum Cells with Application to Logic Synthesis. , 2017, , .		15
147	CTS2M: concurrent task scheduling and storage management for residential energy consumers under dynamic energy pricing. IET Cyber-Physical Systems: Theory and Applications, 2017, 2, 111-117.	1.9	10
148	Hierarchical resource allocation and consolidation framework in a multi-core server cluster using a Markov decision process model. IET Cyber-Physical Systems: Theory and Applications, 2017, 2, 118-126.	1.9	2
149	Achieving Energy Efficiency in Datacenters by Virtual Machine Sizing, Replication, and Placement. Advances in Computers, 2016, 100, 161-200.	1.2	7
150	Standard cell library based layout characterization and power analysis for 10nm gate-all-around (GAA) transistors. , 2016, , .		5
151	Power-aware virtual machine mapping in the data-center-on-a-chip paradigm. , 2016, , .		1
152	Hybrid TFET-MOSFET circuits: An approach to design reliable ultra-low power circuits in the presence of process variation. , 2016, , .		2
153	Efficient Peak Shaving in a Data Center by Joint Optimization of Task Assignment and Energy Storage Management. , 2016, , .		1
154	A Profit Optimization Framework of Energy Storage Devices in Data Centers: Hierarchical Structure and Hybrid Types. , 2016, , .		0
155	Simulation of NoC power-gating: Requirements, optimizations, and the Agate simulator. Journal of Parallel and Distributed Computing, 2016, 95, 69-78.	2.7	9
156	Layout Optimization for Quantum Circuits with Linear Nearest Neighbor Architectures. IEEE Circuits and Systems Magazine, 2016, 16, 62-74.	2.6	27
157	Optimizing the Operating Voltage of Tunnel FET-Based SRAM Arrays Equipped with Read/Write Assist Circuitry. , 2016, , .		1
158	Minimizing the energy-delay product of SRAM arrays using a device-circuit-architecture co-optimization framework. , 2016, , .		10
159	Study on the impact of device parameter variations on performance of III-V homojunction and heterojunction tunnel FETs. Solid-State Electronics, 2016, 124, 46-53.	0.8	5
160	A Reinforcement Learning-Based Power Management Framework for Green Computing Data Centers. , 2016, , .		23
161	An efficient timing analysis model for 6T FinFET SRAM using current-based method. , 2016, , .		5
162	Maximizing the performance of NoC-based MPSoCs under total power and power density constraints. , 2016, , .		5

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163	Negotiation-based resource provisioning and task scheduling algorithm for cloud systems. , 2016, , .		7
164	Hierarchical SLA-Driven Resource Management for Peak Power-Aware and Energy-Efficient Operation of a Cloud Datacenter. IEEE Transactions on Cloud Computing, 2016, 4, 222-236.	3.1	20
165	Optimal co-scheduling of HVAC control and battery management for energy-efficient buildings considering state-of-health degradation. , 2016, , .		14
166	Toward a Profitable Grid-Connected Hybrid Electrical Energy Storage System for Residential Use. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1151-1164.	1.9	7
167	Providing Balanced Mapping for Multiple Applications in Many-Core Chip Multiprocessors. IEEE Transactions on Computers, 2016, 65, 3122-3135.	2.4	3
168	Model-Free Reinforcement Learning and Bayesian Classification in System-Level Power Management. IEEE Transactions on Computers, 2016, 65, 3713-3726.	2.4	30
169	Concurrent Task Scheduling and Dynamic Voltage and Frequency Scaling in a Real-Time Embedded System With Energy Harvesting. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1890-1902.	1.9	25
170	Yield and Speedup Improvements in Extensible Processors by Allocating Extra Cycles to Some Custom Instructions. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-25.	1.9	39
171	An efficient temperature dependent hot carrier injection reliability simulation flow. Microelectronics Reliability, 2016, 57, 10-19.	0.9	0
172	A comparative study on performance and reliability of 32-bit binary adders. The Integration VLSI Journal, 2016, 53, 54-67.	1.3	8
173	All-Region Statistical Model for Delay Variation Based on Log-Skew-Normal Distribution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1503-1508.	1.9	17
174	A Near-Optimal Model-Based Control Algorithm for Households Equipped With Residential Photovoltaic Power Generation and Energy Storage Systems. IEEE Transactions on Sustainable Energy, 2016, 7, 77-86.	5.9	104
175	Joint Charge and Thermal Management for Batteries in Portable Systems With Hybrid Power Sources. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 611-622.	1.9	6
176	Reconfigurable Photovoltaic Array Systems for Adaptive and Fault-Tolerant Energy Harvesting. KAIST Research Series, 2016, , 181-209.	1.5	1
177	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 421-433.	2.1	43
178	Energy-Efficient Cache Memories using a Dual-Vt 4T SRAM Cell with Read-Assist Techniques. , 2016, , .		2
179	SEERAD: A High Speed yet Energy-Efficient Rounding-based Approximate Divider. , 2016, , .		29
180	Profit maximization algorithms for utility companies in an oligopolistic energy market with dynamic prices and intelligent users. AIMS Energy, 2016, 4, 119-135.	1.1	2

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181	10nm Gate-length junctionless gate-all-around (JL-GAA) FETs based 8T SRAM design under process variation using a cross-layer simulation. , 2015, , .		4
182	Power-Efficient Control of Thermoelectric Coolers Considering Distributed Hot Spots. , 2015, , .		3
183	A Thermal Stress-Aware Algorithm for Power and Temperature Management of MPSoCs. , 2015, , .		3
184	Accurate Electrothermal Modeling of Thermoelectric Generators. , 2015, , .		7
185	A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages. International Journal of Circuit Theory and Applications, 2015, 43, 2011-2024.	1.3	7
186	Flexible Prime-Field Genus 2 Hyperelliptic Curve Cryptography Processor with Low Power Consumption and Uniform Power Draw. ETRI Journal, 2015, 37, 107-117.	1.2	3
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