Yoshihiro Hayashi

List of Publications by Year
in descending order

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65	856	567281	580821
papers	citations	15	25
		h-index	g-index

65	65	65	647
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps. , 2010, , .		102
2	Sol-gel derived PbTiO3. Journal of Materials Science, 1987, 22, 2655-2660.	3.7	71
3	Preparation of rod-shaped BaTiO3 powder. Journal of Materials Science, 1986, 21, 757-762.	3.7	66
4	A Novel Variable Inductor Using a Bridge Circuit and Its Application to a 5â€“20 GHz Tunable LC-VCO. IEEE Journal of Solid-State Circuits, 2011, 46, 883-893.	5.4	51
5	Preparation of acicular NiZn-ferrite powders. Journal of Materials Science, 1986, 21, 2876-2880.	3.7	49
6	13.4 A 6.3mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network. , 2015, , .		41
7	Ammonium-Salt-Added Silica Slurry for the Chemical Mechanical Polishing of the Interlayer Dielectric Film Planarization in ULSI's. Japanese Journal of Applied Physics, 1995, 34, 1037-1042.	1.5	37
8	Synthesis and Characterization of Lead-Titanium Complex Alkoxide. Journal of the American Ceramic Society, 1989, 72, 1660-1663.	3.8	35
9	Chemical Structure Effects of Ring-Type Siloxane Precursors on Properties of Plasma-Polymerized Porous SiOCH Films. Journal of the Electrochemical Society, 2007, 154, D354.	2.9	33
10	Improving Reliability of Copper Dual-Damascene Interconnects by Impurity Doping and Interface Strengthening. IEEE Transactions on Electron Devices, 2007, 54, 1867-1877.	3.0	30
11	A 27% Active-Power-Reduced 40-nm CMOS Multimedia SoC With Adaptive Voltage Scaling Using Distributed Universal Delay Lines. IEEE Journal of Solid-State Circuits, 2012, 47, 832-840.	5.4	25
12	Comprehensive Chemistry Designs in Porous SiOCH Film Stacks and Plasma Etching Gases for Damageless Cu Interconnects in Advanced ULSI Devices. IEEE Transactions on Semiconductor Manufacturing, 2008, 21, 469-480.	1.7	23
13	Performance Modeling of Low-k/Cu Interconnects for 32-nm-Node and Beyond. IEEE Transactions on Electron Devices, 2009, 56, 1852-1861.	3.0	22
14	Impact of Barrier Metal Sputtering on Physical and Chemical Damages in Low-kSiOCH Films with Various Hydrocarbon Content. Japanese Journal of Applied Physics, 2008, 47, 2468-2472.	1.5	21
15	Multi-Step Word-Line Control Technology in Hierarchical Cell Architecture for Scaled-Down High-Density SRAMs. IEEE Journal of Solid-State Circuits, 2011, 46, 806-814.	5.4	21
16	Mechanical Property Control of Low-kDielectrics for Diminishing Chemical Mechanical Polishing (CMP)-Related Defects in Cu-Damascene Interconnects. Japanese Journal of Applied Physics, 2004, 43, 1807-1812.	1.5	20
17	Effective 3D open-channel nanostructures of a MgMn₂O₄ positive electrode for rechargeable Mg batteries operated at room temperature. Journal of Materials Chemistry A, 2021, 9, 6851-6860.	10.3	19
18	Feasibility Study of 45-nm-Node Scaled-Down Cu Interconnects With Molecular-Pore-Stacking (MPS) SiOCH Films. IEEE Transactions on Electron Devices, 2007, 54, 797-806.	3.0	13

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19	Mechanism of Ni-Zn Ferrite Formation in the Presence of Molten Li2SO4-Na2SO4. Journal of the American Ceramic Society, 1986, 69, 322-325.	3.8	12
20	Robust Cu Dual Damascene Interconnects With Porous SiOCH Films Fabricated by Low-Damage Multi-Hard-Mask Etching Technology. IEEE Transactions on Semiconductor Manufacturing, 2006, 19, 455-464.	1.7	12
21	Ultrauniform Chemical Mechanical Polishing (CMP) Using a â€œHydro Chuckâ€, Featured by Wafer Mounting on a Quartz Glass Plate with Fully Flat, Water-Supported Surface. Japanese Journal of Applied Physics, 1996, 35, 1054-1059.	1.5	10
22	Effects of the Metallurgical Properties of Upper Cu Film on Stress-Induced Voiding (SIV) in Cu Dual-Damascene Interconnects. Japanese Journal of Applied Physics, 2005, 44, 2294-2302.	1.5	10
23	Characterization of Low-k/Cu Damascene Structures Using Monoenergetic Positron Beams. Japanese Journal of Applied Physics, 2009, 48, 120222.	1.5	10
24	A low-power, small area quadrature LC-VCO using miniature 3D solenoid shaped inductor. , 2009, , .		10
25	Defectless Monolithic Low-k/Cu Interconnects Produced by Chemically Controlled Chemical Mechanical Polishing Process withIn situEnd-Point-Detection Technique. Japanese Journal of Applied Physics, 2009, 48, 04C029.	1.5	9
26	Analysis of Processing Damage on a Ferroelectric SrBi2Ta2O9Capacitor for Ferroelectric Random Access Memory Device Fabrication. Japanese Journal of Applied Physics, 2001, 40, 2341-2347.	1.5	8
27	Smart Fabrication Process of an Ir-IrO[sub x] Top-Electrode on a PZT Film for Reliable FeRAM. Journal of the Electrochemical Society, 2004, 151, G113.	2.9	7
28	Robust Low Oxygen Content Cu Alloy for Scaled-Down ULSI Interconnects Based on Metallurgical Thermodynamic Principles. IEEE Transactions on Electron Devices, 2009, 56, 1579-1587.	3.0	7
29	Porous Low-kImpacts on Performance of Advanced LSI Devices with GHz Operations. Japanese Journal of Applied Physics, 2009, 48, 04C031.	1.5	6
30	Precise Taper-Angle-Control of Via Holes for Reliable Scaled-Down Low-k/Cu Interconnects. Japanese Journal of Applied Physics, 2010, 49, 04DB04.	1.5	6
31	Stabilizing Schemes for the Minority Failure Bits in Ta₂O₅-Based ReRAM Macro. IEEE Transactions on Electron Devices, 2017, 64, 419-426.	3.0	6
32	Nitride-Masked Polishing (NMP) Technique for Surface Planarization of Interlayer-Dielectric Films. Japanese Journal of Applied Physics, 1993, 32, 1060-1063.	1.5	5
33	Multilevel Aluminum Dual-Damascene Interconnects for Process-Step Reduction in 0.18 Âµm ULSIs. Japanese Journal of Applied Physics, 1999, 38, 2360-2367.	1.5	5
34	A Novel Monitoring Method of RF Characteristics Variations for Sub-0.1μm MOSFETs with Precise Gate-resistance Model. , 2006, , .		5
35	Surface Control of Bottom Electrode in Ultra-Thin SiN Metalâ€“Insulatorâ€“Metal Decoupling Capacitors for High Speed Processors. Japanese Journal of Applied Physics, 2007, 46, 1968-1973.	1.5	5
36	Microstructure Control of Low-Loss Niâ€“Zn Ferrite by Low-Temperature Sputtering for On-Chip Magnetic Film. Japanese Journal of Applied Physics, 2009, 48, 04C030.	1.5	5

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37	Improvement of Uniformity and Reliability of Scaled-Down Cu Interconnects with Carbon-Rich Low-kFilms. Japanese Journal of Applied Physics, 2011, 50, 04DB02.	1.5	5
38	Fast voltage control scheme with adaptive voltage control steps and temporary reference voltage overshoots for dynamic voltage and frequency scaling. , 2008, , .		4
39	Via-Shape-Control for Copper Dual-Damascene Interconnects With Low-k Organic Film. IEEE Transactions on Semiconductor Manufacturing, 2008, 21, 256-262.	1.7	4
40	Damascene Cu-interconnect formation in benzocyclobuten (BCB) film using a novel end-point monitoring technique. , 1998, 3508, 30.		3
41	Thermal Stress Control in Cu Dual Damascene Interconnects with Low-k Organic Polymer Film. Journal of the Electrochemical Society, 2010, 157, H1071.	2.9	3
42	A 5–20GHz tunable LC-VCO using variable bridge inductor. , 2010, , .		3
43	A Robust Low-k/Cu Dual Damascene Interconnect (DDI) With Sidewall Protection Layer (SPL). IEEE Transactions on Device and Materials Reliability, 2011, 11, 98-105.	2.0	3
44	Barrier layerless submicron aluminumâ€damascene interconnection using aluminum chemical vapor deposition with a new nucleation method. Electronics and Communications in Japan, 1996, 79, 88-96.	0.2	2
45	A low power LNA using miniature 3D inductor without area penalty of passive components. , 2010, , .		2
46	Scalability study of ultra-thin-body SOI-MOSFETs using full-band and quantum mechanical based device simulation. , 2010, , .		2
47	Improvement of Uniformity and Reliability of Scaled-Down Cu Interconnects with Carbon-Rich Low-kFilms. Japanese Journal of Applied Physics, 2011, 50, 04DB02.	1.5	2
48	Structural Evolution in LSI Devices Reducing Parasitic Effects toward RF/ubiquitous Applications. , 2006, , .		1
49	Extrasmall-Area Three-Dimensional Solenoid-Shaped Inductor Integrated into High-Speed Signal Processing Complementary Metalâ€“Oxideâ€“Semiconductor Ultralarge-Scale Integrated Circuits. Japanese Journal of Applied Physics, 2008, 47, 2477-2483.	1.5	1
50	A Novel Gate Electrode Structure for Reduction of Gate Resistance of Sub-0.1 Âµm RF/Mixed-Signal Metal Oxide Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 04C028.	1.5	1
51	Adding Physical Scalability to BSIM4 by Meta-Modeling of Fitting Parameters. , 2009, , .		1
52	A novel small capacitance RF-MOSFET with small-resistance Long-finger Gate Electrode. , 2010, , .		1
53	Material and Structure Designs for Reliable Quad-Flat-Package for Scaled-Down Ultralarge-Scale Integrations With Porous Low-$k/{m Cu}$ Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 384-390.	2.5	1
54	Molecular-level Manipulation Technology for Low-k Dielectrics Controlling the Physical and Chemical Structures toward 32nm-node BEOLs. Materials Research Society Symposia Proceedings, 2008, 1079, 1.	0.1	0

#	Article	IF	Citations
55	Low-k Dielectrics. , 2009, , 325-342.		0
56	A novel small capacitance RF-MOSFET with small-resistance long-finger gate electrode. , 2010, , .		0
57	A New Differential-Amplifier-Based Offset-Cancellation Sense Amplifier for Speed-Improvement of High-Density Static Random Access Memories in Scaled-Down Complementary Metalâ€“Oxideâ€“Semiconductor Technology. Japanese Journal of Applied Physics, 2010, 49, 04DE09.	1.5	0
58	A Novel Multilayered Niâ€“Zn-Ferrite/TaN Film for RF/Mobile Applications. Japanese Journal of Applied Physics, 2010, 49, 04DB15.	1.5	0
59	Basic Performance of a Logic Intellectual Property Compatible Embedded Dynamic Random Access Memory with Cylinder Capacitors in Low-k/Cu Back End on the Line Layers. Japanese Journal of Applied Physics, 2012, 51, 02BB01.	1.5	0
60	Effects of Low-k Stack Structure on Performance of Complementary Metal Oxide Semiconductor Devices and Chip Package Interaction Failure. Japanese Journal of Applied Physics, 2012, 51, 096504.	1.5	0
61	Lithography for Cu Damascene Fabrication. , 2009, , 299-310.		0
62	Basic Performance of a Logic Intellectual Property Compatible Embedded Dynamic Random Access Memory with Cylinder Capacitors in Low-k/Cu Back End on the Line Layers. Japanese Journal of Applied Physics, 2012, 51, 02BB01.	1.5	0
63	Effects of Low-kStack Structure on Performance of Complementary Metal Oxide Semiconductor Devices and Chip Package Interaction Failure. Japanese Journal of Applied Physics, 2012, 51, 096504.	1.5	0
64	CMP. , 1998, , 414-425.		0
65	Preparation of conductive Cu1.5Mn1.5O4 and Mn3O4 spinel mixture powders as positive active materials in rechargeable Mg batteries operative at room temperature. Journal of Sol-Gel Science and Technology, 0, , .	2.4	0