Hiroyuki Ota

List of Publications by Year
in descending order

140	1,818	394421	414414
papers	citations	19 h-index	32 g-index

140	140	140	1684
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Enhancement of ferroelectricity in sputtered HZO thin films by catalytically generated atomic hydrogen treatment. Japanese Journal of Applied Physics, 2022, 61, SH1004.	1.5	2
2	Wake-up-free properties and high fatigue resistance of HfxZr1â^'xO2-based metalâ€“ferroelectricâ€“semiconductor using top ZrO2 nucleation layer at low thermal budget (300â€‰Â°C). APL Materials, 2022, 10, .	5.1	14
3	Thermal stability of ferroelectricity in hafniumâ€“zirconium dioxide films deposited by sputtering and chemical solution deposition for oxide-channel ferroelectric-gate transistor applications. Applied Physics Express, 2021, 14, 041006.	2.4	6
4	Accelerated ferroelectric phase transformation in HfO₂/ZrO₂ nanolaminates. Applied Physics Express, 2021, 14, 051006.	2.4	15
5	Impact of reduced pressure crystallization on ferroelectric properties in hafnium-zirconium dioxide films deposited by sputtering. Japanese Journal of Applied Physics, 2021, 60, SFFB05.	1.5	8
6	Investigation of the wake-up process and time-dependent imprint of Hf0.5Zr0.5O2 film through the direct piezoelectric response. Applied Physics Letters, 2021, 119, .	3.3	6
7	Device simulation of negative-capacitance field-effect transistors with a uniaxial ferroelectric gate insulator. Nonlinear Theory and Its Applications IEICE, 2020, 11, 145-156.	0.6	1
8	Design points of ferroelectric field-effect transistors for memory and logic applications as investigated by metal-ferroelectric-metalâ€“insulatorâ€“semiconductor gate stack structures using Hf_{0.5}Zr_{0.5}O₂ films. Japanese Journal of Applied Physics, 2019, 58, SLLB06.	1.5	6
9	Phase transformation behavior of ultrathin Hf_{0.5}Zr_{0.5}O₂ films investigated through wide range annealing experiments. Japanese Journal of Applied Physics, 2019, 58, SBBA07.	1.5	38
10	A TCAD device simulator for exotic materials and its application to a negative-capacitance FET. Journal of Computational Electronics, 2019, 18, 534-542.	2.5	19
11	Polarization switching behavior of Hfâ€“Zrâ€“O ferroelectric ultrathin films studied through coercive field characteristics. Japanese Journal of Applied Physics, 2018, 57, 04FB01.	1.5	79
12	Simulation study of short-channel effects of tunnel field-effect transistors. Japanese Journal of Applied Physics, 2018, 57, 04FD04.	1.5	3
13	Design of steep-slope negative-capacitance FinFETs for dense integration: Importance of appropriate ferroelectric capacitance and short-channel effects. Japanese Journal of Applied Physics, 2018, 57, 04FD03.	1.5	2
14	Fringing field effects in negative capacitance field-effect transistors with a ferroelectric gate insulator. Japanese Journal of Applied Physics, 2018, 57, 04FD07.	1.5	16
15	Device Simulation of Negative-Capacitance Field-Effect Transistors With a Ferroelectric Gate Insulator. , 2018, , .		3
16	On the drain bias dependence of long-channel silicon-on-insulator-based tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD04.	1.5	2
17	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
18	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2

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19	Impacts of plasma-induced damage due to UV light irradiation during etching on Ge fin fabrication and device performance of Ge fin field-effect transistors. Applied Physics Express, 2017, 10, 026501.	2.4	33
20	Thickness-independent behavior of coercive field in HfO<inf>2</inf>-based ferroelectrics. , 2017, , .		6
21	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
22	Perspective of negative capacitance FinFETs investigated by transient TCAD simulation. , 2017, , .		17
23	Structural advantages of silicon-on-insulator FETs over FinFETs in steep subthreshold-swing operation in ferroelectric-gate FETs. Japanese Journal of Applied Physics, 2017, 56, 04CD10.	1.5	9
24	Interlayer coupling effect on the performance of monolithic three-dimensional inverters and its dependence on the interlayer dielectric thickness. Japanese Journal of Applied Physics, 2017, 56, 04CC02.	1.5	4
25	First Experimental Observation of Channel Thickness Scaling Induced Electron Mobility Enhancement in UTB-GeOI nMOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 4615-4621.	3.0	15
26	Design and simulation of steep-slope silicon-on-insulator FETs using negative capacitance: Impact of buried oxide thickness and remnant polarization. , 2016, , .		1
27	Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration. , 2016, , .		77
28	Material and device engineering in fully depleted silicon-on-insulator transistors to realize a steep subthreshold swing using negative capacitance. Japanese Journal of Applied Physics, 2016, 55, 08PD01.	1.5	20
29	Steep subthreshold swing and energy efficiency in MOSFFETs utilizing nonlinear gate dielectric insulators. Japanese Journal of Applied Physics, 2016, 55, 04ED02.	1.5	2
30	(Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24.	0.5	1
31	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
32	Gate-First High-Performance Germanium nMOSFET and pMOSFET Using Low Thermal Budget Ion Implantation After Germanidation Technique. IEEE Electron Device Letters, 2016, 37, 253-256.	3.9	25
33	Achieving low parasitic resistance in Ge p-channel metalâ€“oxideâ€“semiconductor field-effect transistors by ion implantation after germanidation. Applied Physics Express, 2015, 8, 054201.	2.4	11
34	Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06.	1.5	4
35	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7
36	Design guidelines to achieve minimum energy operation for ultra low voltage tunneling FET logic circuits. Japanese Journal of Applied Physics, 2015, 54, 04DC04.	1.5	15

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37	Effect of hot implantation on ON-current enhancement utilizing isoelectronic trap in Si-based tunnel field-effect transistors. Applied Physics Express, 2015, 8, 036503.	2.4	9
38	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
39	Study of gate leakage current paths in p-channel tunnel field-effect transistor by current separation measurement and device simulation. Japanese Journal of Applied Physics, 2015, 54, 034202.	1.5	1
40	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
41	Study of tunneling transport in Si-based tunnel field-effect transistors with ON current enhancement utilizing isoelectronic trap. Applied Physics Letters, 2015, 106, .	3.3	54
42	Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04.	1.5	2
43	Comparative Study of Charge Trapping Type SOI-FinFET Flash Memories with Different Blocking Layer Materials. Journal of Low Power Electronics and Applications, 2014, 4, 153-167.	2.0	5
44	Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201.	2.4	35
45	Operation of inverter and ring oscillator of ultrathin-body poly-Ge CMOS. Applied Physics Express, 2014, 7, 121302.	2.4	29
46	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4
47	Band-to-band tunneling current enhancement utilizing isoelectronic trap and its application to TFETs. , 2014, , .		22
48	Importance of interface engineering for synthesis of SrHfO₃ perovskite thin films on Si substrates through crystallization of amorphous films and control of flat-band voltages of metalâ€“oxideâ€“semiconductor capacitors. Japanese Journal of Applied Physics, 2014, 53, 04EA03.	1.5	4
49	Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11.	1.5	12
50	Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16.	1.5	2
51	(Invited) Charge Trapping Type SOI-FinFET Flash Memory. ECS Transactions, 2014, 61, 263-280.	0.5	4
52	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
53	Predictivity of the non-local BTBT model for structure dependencies of tunnel FETs. , 2014, , .		9
54	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7

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55	Experimental Demonstration of Ultrashort-Channel (3 nm) Junctionless FETs Utilizing Atomically Sharp V-Grooves on SOI. IEEE Nanotechnology Magazine, 2014, 13, 208-215.	2.0	59
56	Experimental study of charge trapping type FinFET flash memory. , 2014, , .		0
57	Variability of short channel junctionless field-effect transistors caused by fluctuation of dopant concentration. , 2013, , .		1
58	Two-step annealing effects on ultrathin EOT higher-k (k=40) ALD-HfO2 gate stacks. Solid-State Electronics, 2013, 84, 58-64.	1.4	11
59	A compact model for tunnel field-effect transistors incorporating nonlocal band-to-band tunneling. Journal of Applied Physics, 2013, 114, 144512.	2.5	25
60	Tunnel Field-Effect Transistor with Epitaxially Grown Tunnel Junction Fabricated by Source/Drain-First and Tunnel-Junction-Last Processes. Japanese Journal of Applied Physics, 2013, 52, 04CC25.	1.5	16
61	(Invited) Extremely Short Channel Si-MOSFETs Prepared on SOI Substrates Using Anisotropic Wet Etching. ECS Transactions, 2013, 58, 273-280.	0.5	0
62	Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, .	3.3	15
63	Fabrication and Demonstration of 3-nm-Channel-Length Junctionless Field-Effect Transistors on Silicon-on-Insulator Substrates Using Anisotropic Wet Etching and Lateral Diffusion of Dopants. Japanese Journal of Applied Physics, 2013, 52, 04CA01.	1.5	21
64	Extremely Scaled (${sim}0.2$ nm) Equivalent Oxide Thickness of Higher-k ($k = 40$) HfO$_{2}$ Gate Stacks Prepared by Atomic Layer Deposition and Oxygen-Controlled Cap Post-Deposition Annealing. Japanese Journal of Applied Physics, 2012, 51, 02BA04.	1.5	4
65	Simultaneous flattening of Si(110), (111), and (001) surfaces for three-dimensional Si nanowires. Applied Physics Letters, 2012, 100, 261605.	3.3	4
66	Two-step annealing effects on ultrathin EOT higher-k (k = 40) ALD-HfO<inf>2</inf> gate stacks. , 2012, , .		0
67	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	0
68	Extremely Scaled Equivalent Oxide Thickness of High-k (k=40) HfO2 Gate Stacks Prepared by Atomic Layer Deposition and Ti Cap Anneal. Hyomen Kagaku, 2012, 33, 610-615.	0.0	0
69	Suppressing V<inf>t</inf> and G<inf>m</inf> variability of FinFETs using amorphous metal gates for 14 nm and beyond. , 2012, , .		22
70	Exact control of junction position using epitaxial NiSi2 crystallization in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect transistors. AIP Advances, 2012, 2, .	1.3	1
71	Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010.	3.0	27
72	Extremely Scaled (âˆ¼0.2 nm) Equivalent Oxide Thickness of Higher-k(k= 40) HfO2Gate Stacks Prepared by Atomic Layer Deposition and Oxygen-Controlled Cap Post-Deposition Annealing. Japanese Journal of Applied Physics, 2012, 51, 02BA04.	1.5	7

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73	(Invited) Epitaxial HfO₂ Thin Films on Si Substrates: Strategy for Sub-1 nm EOT Technology. ECS Transactions, 2011, 41, 135-144.	0.5	3
74	Nature of interface traps in Ge metal-insulator-semiconductor structures with GeO2 interfacial layers. Journal of Applied Physics, 2011, 109, .	2.5	18
75	Accurate evaluation of Ge metalâ€"insulatorâ€"semiconductor interface properties. Journal of Applied Physics, 2011, 110, .	2.5	14
76	Observation of Work Functions, Metallicity, Band Bending, Interfacial Dipoles by EUPS for Characterizing High-kâˆ•Metal Interfaces. AIP Conference Proceedings, 2011, , .	0.4	7
77	Fabrication of Direct-Contact Higher-k HfO₂ Gate Stacks by Oxygen-Controlled Cap Post-Deposition Annealing. Japanese Journal of Applied Physics, 2011, 50, 10PG01.	1.5	14
78	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	7
79	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	13
80	Fabrication of Direct-Contact Higher-kHfO₂Gate Stacks by Oxygen-Controlled Cap Post-Deposition Annealing. Japanese Journal of Applied Physics, 2011, 50, 10PG01.	1.5	5
81	Fabrication of High-k Gate Insulator Films by Atomic Layer Deposition and Their Properties Influenced by Substrate Hydrophilicity. Journal of the Vacuum Society of Japan, 2011, 54, 105-109.	0.3	0
82	AFM measurement of atomic-scale Si surface etching by active oxidation. Surface Science, 2010, 604, 1432-1437.	1.9	6
83	Effect of Ge Metalâ€"Insulatorâ€"Semiconductor Interfacial Layers on Interface Trap Density near the Conduction Band Edge. Japanese Journal of Applied Physics, 2010, 49, 04DA09.	1.5	3
84	Physical origins of mobility enhancement of Ge p-channel metal-insulator-semiconductor field effect transistors with Si passivation layers. Journal of Applied Physics, 2010, 108, 104511.	2.5	20
85	Effect of Al-diffusion-induced positive flatband voltage shift on the electrical characteristics of Al-incorporated high-k metal-oxide-semiconductor field-effective transistor. Journal of Applied Physics, 2009, 105, 064108.	2.5	16
86	Application of Advanced Atomic Layer Deposition for Understanding and Control of VTH and EOT in Metal/High-k Gate Stacks. ECS Transactions, 2009, 16, 69-75.	0.5	0
87	Design of High-k Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing Method. ECS Transactions, 2009, 19, 129-143.	0.5	2
88	Structural Metastability and Size Scalability of Phase-Controlled HfO2 Formed through Cap-PDA. ECS Transactions, 2009, 19, 563-575.	0.5	7
89	Inversion Layer Mobility in High-k Dielectric MOSFETs - Intrinsic Mobility Degradation by Electric Dipoles at High-k/SiO2 Interface. ECS Transactions, 2009, 16, 67-75.	0.5	0
90	Impact of Surface Hydrophilicization prior to Atomic Layer Deposition for HfO₂/Si Direct-Contact Gate Stacks. Applied Physics Express, 2009, 2, 011201.	2.4	16

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91	Metal carbide-induced negative flatband voltage shift in TaCx and HfCx/HfO2 gate stacks. Applied Surface Science, 2008, 254, 6123-6126.	6.1	1
92	Changes in effective work function of HfxRu1âˆ’x alloy gate electrode. Microelectronic Engineering, 2008, 85, 1524-1528.	2.4	14
93	Experimental evidence for the flatband voltage shift of high-k metal-oxide-semiconductor devices due to the dipole formation at the high-kâ•SiO2 interface. Applied Physics Letters, 2008, 92, .	3.3	140
94	Roles of high-k and interfacial layers on TDDB reliability studied with HfAlO<inf>X</inf>/SiO<inf>2</inf> stacked gate dielectrics. , 2008, , .		4
95	TDDB and BTI reliabilities of high-k stacked gate dielectrics - Impact of initial traps in high-k layer -. , 2008, , .		1
96	Separation of fast and slow NBTI components under long-term stress in pMISFETs with ultra-thin high-k and SiON dielectrics. , 2008, , .		0
97	What is the Essence of VFB Shifts in High-k Gate Stack?. ECS Transactions, 2007, 11, 543-555.	0.5	16
98	Achievement of Higher-k and High-Î¦ in Phase Controlled HfO2 Film Using Post Gate Electrode Deposition Annealing. ECS Transactions, 2007, 11, 35-45.	0.5	18
99	Gate-First Processed FUSI/HfO<inf>2</inf>/HfSiO<inf>x</inf>/Si MOSFETs with EOT=0.5 nm - Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing. , 2007, , .		8
100	Materials Science-based Device Performance Engineering for Metal Gate High-k CMOS. , 2007, , .		8
101	Intrinsic Origin of Electron Mobility Reduction in High-k MOSFETs - From Remote Phonon to Bottom Interface Dipole Scattering. , 2007, , .		22
102	Comprehensive Study of V<inf>FB</inf> Shift in High-k CMOS - Dipole Formation, Fermi-level Pinning and Oxygen Vacancy Effect. , 2007, , .		39
103	Reliability Perspective of High-k Gate Stack Assessed by Temperature Dependence of Dielectric Breakdown. , 2007, , .		5
104	V<inf>FB</inf> Roll-off in HfO<inf>2</inf> Gate Stack after High Temperature Annealing Process - A Crucial Role of Out-diffused Oxygen from HfO<inf>2</inf> to Si. , 2007, , .		13
105	Dielectric Breakdown in High-K Gate Dielectrics - Mechanism and Lifetime Assessment. , 2007, , .		23
106	0.6nm-EOT high-k gate stacks with HfSiOx interfacial layer grown by solid-phase reaction between HfO2 and Si substrate. Microelectronic Engineering, 2007, 84, 1861-1864.	2.4	30
107	Mechanism of Gradual Increase of Gate Current in High-K Gate Dielectrics and Its Application to Reliability Assessment. , 2006, , .		9
108	Low-Threshold-Voltage HfOxN p-Channel Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors with Partially Silicided Platinum Gate Electrode. Japanese Journal of Applied Physics, 2006, 45, 6225-6230.	1.5	5

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109	Symmetrical threshold voltage in complementary metal-oxide-semiconductor field-effect transistors with HfAlOx(N) achieved by adjusting Hfâˆ•Al compositional ratio. Journal of Applied Physics, 2006, 99, 054506.	2.5	21
110	Advantages of HfAlON gate dielectric film for advanced low power CMOS application. Microelectronic Engineering, 2005, 80, 190-197.	2.4	18
111	Carrier separation analysis for clarifying carrier conduction and degradation mechanisms in high-k stack gate dielectrics. Microelectronics Reliability, 2005, 45, 1041-1050.	1.7	9
112	Weak Temperature Dependence of Non-Coulomb Scattering Component of HfAlOx-Limited Inversion Layer Mobility in n+-Polysilicon/HfAlOx/SiO2N-Channel Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2005, 44, 7750-7755.	1.5	10
113	Study on Oxynitride Buffer Layers in HfO2Metalâ€“Insulatorâ€“Semiconductor Structures for Improving Metalâ€“Insulatorâ€“Semiconductor Field-Effect Transistor Performance. Japanese Journal of Applied Physics, 2005, 44, 1698-1703.	1.5	6
114	Degradation mechanism of HfAlOXâˆ•SiO2 stacked gate dielectrics studied by transient and steady-state leakage current analysis. Journal of Applied Physics, 2005, 97, 074505.	2.5	6
115	Correlation between scanning-probe-induced spots and fixed positive charges in thin HfO2 films. Applied Physics Letters, 2005, 86, 112906.	3.3	9
116	Roles of nitrogen incorporation in HfAlO[sub x](N) gate dielectrics for suppression of boron penetration. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2004, 22, 2128.	1.6	9
117	Effect of the interfacial SiO2 layer thickness on the dominant carrier type in leakage currents through HfAlOxâˆ•SiO2 gate dielectric films. Applied Physics Letters, 2004, 85, 6227-6229.	3.3	7
118	Fabrication and electrical properties of ferroelectric-gate FETS with epitaxial gate structures. Electronics and Communications in Japan, 2004, 87, 24-33.	0.2	0
119	Memory properties of a ferroelectric gate field-effect transistor with an adjoining metalâ€“ferroelectricâ€“metal assistance cell. Journal of Applied Physics, 2003, 94, 2559-2562.	2.5	14
120	Fabrication and critical currents of thin-film-type Bi2Sr2CaCu2Ox intrinsic Josephson junctions. Physica C: Superconductivity and Its Applications, 2001, 362, 256-260.	1.2	10
121	Fabrication and Electrical Characteristics of a Trench-Type Metal-Ferroelectric-Metal-Insulator-Semiconductor Field Effect Transistor. Japanese Journal of Applied Physics, 2001, 40, 5605-5609.	1.5	1
122	All-perovskite-oxide ferroelectric memory transistor composed of Bi2Sr2CuOx and PbZr0.5Ti0.5O3 films. Journal of Applied Physics, 2001, 89, 8153-8158.	2.5	13
123	Epitaxial structure SrBi2Ta2O9<116> /SrTiO3<011> /Ce0.12Zr0.88O2<001> /Si<001> for ferroelectric-gate FET memory. Integrated Ferroelectrics, 2001, 40, 135-143.	0.7	5
124	Epitaxial Growth of Bi4Ti3O12/CeO2/Ce0.12Zr0.88O2and Bi4Ti3O12/SrTiO3/Ce0.12Zr0.88O2Thin Films on Si and Its Application to Metal-Ferroelectric-Insulator-Semiconductor Diodes. Japanese Journal of Applied Physics, 2000, 39, 5505-5511.	1.5	6
125	Particle-free superconducting Bi2Sr2CaCu2Ox ultrathin films prepared by atomic-layer-controlled molecular beam epitaxy technique. Physica C: Superconductivity and Its Applications, 1999, 311, 42-48.	1.2	14
126	Charge and vortex Kosterlitzâ€“Thouless transitions in Bi-superconducting mixed crystal thin films. Physica C: Superconductivity and Its Applications, 1999, 317-318, 661-665.	1.2	2

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127	Epitaxial Bi4Ti3O12 thin film growth using Bi self-limiting function. Journal of Crystal Growth, 1999, 200, 161-168.	1.5	24
128	Pulsed laser deposition and ferroelectric properties of SrBi2Ta2O9 thin films. Materials Letters, 1999, 38, 406-412.	2.6	12
129	Molecular beam epitaxial growth of BSCCO and Bi-based oxides: self-limiting growth of the Bi element. , 1998, , .		0
130	Formation of phase intergrowth in the syntheses of Bi-superconducting thin films. Applied Physics Letters, 1997, 70, 1471-1473.	3.3	25
131	Self-limiting process for the bismuth content in molecular beam epitaxial growth of Bi2Sr2CuOy thin films. Applied Physics Letters, 1997, 71, 3712-3714.	3.3	36
132	Superstructure observation on a MgO(100) surface. Surface Science, 1996, 357-358, 150-154.	1.9	15
133	Sheet resistance in BSCCO thin films with phase intergrowth. European Physical Journal D, 1996, 46, 1375-1376.	0.4	0
134	The influence of Bi-sticking coefficient in the growth of Bi(2212) thin film by ion beam sputtering. Thin Solid Films, 1996, 281-282, 510-512.	1.8	10
135	Comparison between Bi-superconductor thin films fabricated via co-deposition and layer-by-layer deposition by ion beam sputtering method. Thin Solid Films, 1996, 281-282, 517-520.	1.8	6
136	Thermodynamics for formation of each stable single phase in BSCCO thin films. Journal of Low Temperature Physics, 1996, 105, 1283-1288.	1.4	6
137	Surface morphology for annealed and etched MgO(100). Journal of Low Temperature Physics, 1996, 105, 1343-1348.	1.4	19
138	Carrier separation analysis for clarifying leakage mechanism in unstressed and stressed HfAlO/sub x//SiO/sub 2/ stack dielectric layers. , 0, , .		2
139	Partial silicides technology for tunable work function electrodes on high-k gate dielectrics - fermi level pinning controlled PtS/sub X/, for HfO/sub X/(N) pMOSFET. , 0, , .		15
140	Model for dielectric breakdown mechanism of HfAlO/sub X//SiO/sub 2/ stacked gate dielectrics dominated by the generated subordinate carrier injection. , 0, , .		3