Jia-Fei Yao

List of Publications by Year
in descending order

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28 papers	208 citations	1478505 6 h-index	1058476 14 g-index
28 all docs	28 docs citations	28 times ranked	122 citing authors

#	Article	IF	Citations
1	A 2.2kV Organic Semiconductor- Based Lateral Power Device. IEEE Electron Device Letters, 2022, 43, 276-279.	3.9	5
2	Field Plate-Adaptive Doping: A Novel Surface Electric Field Optimization Technique for SOI LDMOS With Gate Field Plate. IEEE Transactions on Electron Devices, 2022, 69, 291-297.	3.0	3
3	Extraction of Interface-Trap Densities of the Stacked Bonding Structure in 3D Integration Using High-Frequency Capacitance-Voltage Technique. Micromachines, 2022, 13, 262.	2.9	0
4	Î²-Ga2O3-Based Power Devices: A Concise Review. Crystals, 2022, 12, 406.	2.2	34
5	Prediction of Static Characteristic Parameters of an Insulated Gate Bipolar Transistor Using Artificial Neural Network. Micromachines, 2022, 13, 4.	2.9	5
6	Off-State Performance Characterization of an AlGaN/GaN Device via Artificial Neural Networks. Micromachines, 2022, 13, 737.	2.9	0
7	Double dielectrics enhancement on the LDMOS using high-k field dielectric and low-k buried dielectric. Results in Physics, 2022, 38, 105599.	4.1	4
8	Deep neural network-based approach for breakdown voltage and specific on-resistance prediction of SOI LDMOS with field plate. Japanese Journal of Applied Physics, 2021, 60, 077002.	1.5	5
9	The Application of the High-k Dielectrics in Lateral Double-Diffused Metal Oxide Semiconductor. , 2021, , .		0
10	Novel LDMOS With Integrated Triple Direction High-k Gate and Field Dielectrics. IEEE Transactions on Electron Devices, 2021, 68, 3997-4003.	3.0	8
11	A Novel Stepâ€“Doped Channel AlGaN/GaN HEMTs with Improved Breakdown Performance. Micromachines, 2021, 12, 1244.	2.9	4
12	3-D analytical model of the high-voltage interconnection effect for SOI LDMOS. Superlattices and Microstructures, 2021, 160, 107056.	3.1	0
13	Analytical Study on the Breakdown Characteristics of Si-Substrated AlGaN/GaN HEMTs With Field Plates. IEEE Journal of the Electron Devices Society, 2020, 8, 1031-1038.	2.1	3
14	An Analytical Breakdown Model for the SOI LDMOS With Arbitrary Drift Doping Profile by Using Effective Substrate Voltage Method. IEEE Journal of the Electron Devices Society, 2020, 8, 49-56.	2.1	5
15	Numerical and analytical investigations for the SOI LDMOS with alternated high-k dielectric and step doped silicon pillars*. Chinese Physics B, 2020, 29, 038503.	1.4	8
16	The New Structure and Analytical Model of a High-Voltage Interconnection Shielding Structure With High-k Dielectric Pillar. IEEE Transactions on Electron Devices, 2020, 67, 1745-1750.	3.0	5
17	Analysis of Interface Properties in AlGaN/GaN MIS-HEMTs with HfO2 and SiNx Gate Dielectric. , 2020, , .		2
18	Analytical Model for the SOI Lateral Power Device With Step Width Technique and High-${k}$ Dielectric. IEEE Transactions on Electron Devices, 2019, 66, 3055-3059.	3.0	9

#	Article	IF	Citations
19	Numerical Analysis of the LDMOS With Side Triangular Field Plate. IEEE Journal of the Electron Devices Society, 2019, 7, 1055-1062.	2.1	6
20	Simulation Study of the Slope-Channel Double-Gate MOSFET for Low-Power Applications. , 2019, , .		1
21	Area-Efficient and Snapback-Free SOI LIGBT With L-Shaped Extraction Path. IEEE Journal of the Electron Devices Society, 2019, 7, 728-734.	2.1	3
22	A Novel High-k LDMOS with Triangular Trench Field Plate. , 2019, , .		1
23	A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 1843-1848.	3.0	6
24	A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout. IEEE Transactions on Electron Devices, 2018, 65, 1447-1452.	3.0	21
25	Performance Variability, Switching Mechanism, and Physical Model for Oxide Based Memristor and RRAM Device. , 2018, , .		3
26	A new RESURF model based on sharing charge gradual apportionment concept for lateral power devices. , 2015, , .		1
27	Novel high-voltage LDMOS with linear graded drift region width. , 2015, , .		2
28	Variation of Lateral Width Technique in SoI High-Voltage Lateral Double-Diffused Metalâ€“Oxideâ€“Semiconductor Transistors Using High-k Dielectric. IEEE Electron Device Letters, 2015, 36, 262-264.	3.9	64