# Tsu-Jae Liu

List of Publications by Year
in descending order

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| 138 | 4,509 | 172457 | 118850 |
|---|---|---|---|
| papers | citations | 29 h-index | 62 g-index |

| 139 | 139 | 139 | 2740 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. IEEE Electron Device Letters, 2007, 28, 743-745. | 3.9 | 1,537 |
| 2 | Demonstration of L-Shaped Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2016, 63, 1774-1778. | 3.0 | 250 |
| 3 | Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off. IEEE Journal of Solid-State Circuits, 2008, 43, 600-609. | 5.4 | 155 |
| 4 | Tunnel Field Effect Transistor With Raised Germanium Source. IEEE Electron Device Letters, 2010, 31, 1107-1109. | 3.9 | 141 |
| 5 | Large-Scale SRAM Variability Characterization in 45 nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 3174-3192. | 5.4 | 133 |
| 6 | Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET. IEEE Electron Device Letters, 2013, 34, 184-186. | 3.9 | 124 |
| 7 | Gate Line Edge Roughness Model for Estimation of FinFET Performance Variability. IEEE Transactions on Electron Devices, 2009, 56, 3055-3063. | 3.0 | 87 |
| 8 | Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET. IEEE Transactions on Electron Devices, 2009, 56, 1538-1542. | 3.0 | 85 |
| 9 | Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages. , 2008, , . | | 72 |
| 10 | Prospect of tunneling green transistor for 0.1V CMOS. , 2010, , . | | 61 |
| 11 | Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. IEEE Electron Device Letters, 2008, 29, 491-493. | 3.9 | 59 |
| 12 | A Comparative Study of Dopant-Segregated Schottky and Raised Source/Drain Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 2665-2677. | 3.0 | 57 |
| 13 | SRAM Read/Write Margin Enhancements Using FinFETs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 887-900. | 3.1 | 57 |
| 14 | Characterization of Dynamic SRAM Stability in 45 nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 2702-2712. | 5.4 | 54 |
| 15 | Nano-Electro-Mechanical Nonvolatile Memory (NEMory) Cell Design and Scaling. IEEE Transactions on Electron Devices, 2008, 55, 3482-3488. | 3.0 | 46 |
| 16 | FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling. IEEE Transactions on Electron Devices, 2015, 62, 3945-3950. | 3.0 | 46 |
| 17 | Germanium Gate PhotoMOSFET Integrated to Silicon Photonics. IEEE Journal of Selected Topics in Quantum Electronics, 2014, 20, 1-7. | 2.9 | 44 |
| 18 | Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes. Journal of Microelectromechanical Systems, 2012, 21, 511-513. | 2.5 | 43 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Mechanically modulated tunneling resistance in monolayer MoS2. Applied Physics Letters, 2013, 103, . | 3.3 | 43 |
| 20 | Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node. IEEE Transactions on Electron Devices, 2010, 57, 1301-1309. | 3.0 | 40 |
| 21 | Perfectly Complementary Relay Design for Digital Logic Applications. IEEE Electron Device Letters, 2010, 31, 371-373. | 3.9 | 40 |
| 22 | Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration. , 2007, , . | | 39 |
| 23 | Effectiveness of Stressors in Aggressively Scaled FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 1592-1598. | 3.0 | 39 |
| 24 | MOSFET design for forward body biasing scheme. IEEE Electron Device Letters, 2006, 27, 387-389. | 3.9 | 38 |
| 25 | ZrO<sub>2</sub> Ferroelectric FET for Non-volatile Memory Application. IEEE Electron Device Letters, 2019, 40, 1419-1422. | 3.9 | 38 |
| 26 | Dopant-Segregated Schottky Source/Drain Double-Gate MOSFET Design in the Direct Source-to-Drain Tunneling Regime. IEEE Transactions on Electron Devices, 2009, 56, 2016-2026. | 3.0 | 37 |
| 27 | Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications. , 2014, , . | | 36 |
| 28 | Seesaw Relay Logic and Memory Circuits. Journal of Microelectromechanical Systems, 2010, 19, 1012-1014. | 2.5 | 35 |
| 29 | Characterization of Polycrystalline Silicon-Germanium Film Deposition for Modularly Integrated MEMS Applications. Journal of Microelectromechanical Systems, 2007, 16, 68-77. | 2.5 | 32 |
| 30 | Impact of Body Doping and Thickness on the Performance of Germanium-Source TFETs. IEEE Transactions on Electron Devices, 2010, 57, 1710-1713. | 3.0 | 32 |
| 31 | Design Optimization of Multigate Bulk MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 28-33. | 3.0 | 31 |
| 32 | Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions. Journal of Microelectromechanical Systems, 2014, 23, 198-203. | 2.5 | 31 |
| 33 | MOSFET hot-carrier reliability improvement by forward-body bias. IEEE Electron Device Letters, 2006, 27, 605-608. | 3.9 | 29 |
| 34 | Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study. IEEE Transactions on Electron Devices, 2009, 56, 1483-1492. | 3.0 | 25 |
| 35 | Simulation-Based Study of the Inserted-Oxide FinFET for Future Low-Power System-on-Chip Applications. IEEE Electron Device Letters, 2015, 36, 742-744. | 3.9 | 25 |
| 36 | Simulation-Based Study of Hybrid Fin/Planar LDMOS Design for FinFET-Based System-on-Chip Technology. IEEE Transactions on Electron Devices, 2017, 64, 4193-4199. | 3.0 | 25 |

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| 37 | Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. IEEE Electron Device Letters, 2012, 33, 318-320. | 3.9 | 24 |
| 38 | Large-scale read/write margin measurement in 45nm CMOS SRAM arrays. , 2008, , . | | 23 |
| 39 | Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits. IEEE Electron Device Letters, 2010, 31, 890-892. | 3.9 | 21 |
| 40 | Design Requirements for Steeply Switching Logic Devices. IEEE Transactions on Electron Devices, 2012, 59, 326-334. | 3.0 | 21 |
| 41 | Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching. IEEE Electron Device Letters, 2016, 37, 31-34. | 3.9 | 20 |
| 42 | A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement. , 2006, , . | | 19 |
| 43 | Dopant-Segregated Schottky Junction Tuning With Fluorine Pre-Silicidation Ion Implant. IEEE Transactions on Electron Devices, 2010, 57, 1084-1092. | 3.0 | 19 |
| 44 | Spacer Gate Lithography for Reduced Variability Due to Line Edge Roughness. IEEE Transactions on Semiconductor Manufacturing, 2010, 23, 311-315. | 1.7 | 19 |
| 45 | Impact of back biasing on carrier transport in ultra-thin-body and BOX (UTBB) Fully Depleted SOI MOSFETs. , 2012, , . | | 19 |
| 46 | Scaling Limitations for Flexural Beams Used in Electromechanical Devices. IEEE Transactions on Electron Devices, 2009, 56, 688-691. | 3.0 | 18 |
| 47 | Planar GeOI TFET Performance Improvement With Back Biasing. IEEE Transactions on Electron Devices, 2012, 59, 1629-1635. | 3.0 | 18 |
| 48 | High-Mobility Ge pMOSFETs With Crystalline ZrO<sub>2</sub> Dielectric. IEEE Electron Device Letters, 2019, 40, 371-374. | 3.9 | 18 |
| 49 | Pull-In and Release Voltage Design for Nanoelectromechanical Field-Effect Transistors. IEEE Transactions on Electron Devices, 2009, 56, 3072-3082. | 3.0 | 17 |
| 50 | Four-Terminal Relay Design for Improved Body Effect. IEEE Electron Device Letters, 2010, 31, 515-517. | 3.9 | 17 |
| 51 | Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic. IEEE Electron Device Letters, 2016, 37, 1563-1565. | 3.9 | 17 |
| 52 | Prospects for MEM logic switch technology. , 2010, , . | | 16 |
| 53 | Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield. IEEE Transactions on Electron Devices, 2014, 61, 2371-2377. | 3.0 | 16 |
| 54 | Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits. IEEE Electron Device Letters, 2012, 33, 281-283. | 3.9 | 15 |

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| 55 | Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. IEEE Transactions on Electron Devices, 2013, 60, 1790-1793. | 3.0 | 15 |
| 56 | Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. IEEE Transactions on Electron Devices, 2014, 61, 3949-3954. | 3.0 | 15 |
| 57 | Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. IEEE Electron Device Letters, 2015, 36, 862-864. | 3.9 | 15 |
| 58 | Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit. IEEE Electron Device Letters, 2015, 36, 963-965. | 3.9 | 15 |
| 59 | Scale-Length Assessment of the Trigate Bulk MOSFET Design. IEEE Transactions on Electron Devices, 2009, 56, 2840-2842. | 3.0 | 14 |
| 60 | A Novel Self-Aligned 4-Bit SONOS-Type Nonvolatile Memory Cell With T-Gate and I-Shaped FinFET Structure. IEEE Transactions on Electron Devices, 2010, 57, 1728-1736. | 3.0 | 14 |
| 61 | Impact of Gate Line-Edge Roughness (LER) Versus Random Dopant Fluctuations (RDF) on Germanium-Source Tunnel FET Performance. IEEE Nanotechnology Magazine, 2013, 12, 1061-1067. | 2.0 | 14 |
| 62 | Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs with Sub-kT/q Swing. IEEE Electron Device Letters, 2018, , 1-1. | 3.9 | 14 |
| 63 | Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage. , 2012, , . | | 13 |
| 64 | Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. IEEE Transactions on Device and Materials Reliability, 2011, 11, 378-386. | 2.0 | 12 |
| 65 | Electromechanical Diode Cell for Cross-Point Nonvolatile Memory Arrays. IEEE Electron Device Letters, 2012, 33, 131-133. | 3.9 | 12 |
| 66 | MOSFET performance and scalability enhancement by insertion of oxygen layers. , 2012, , . | | 12 |
| 67 | The Effect of Random Dopant Fluctuation on Specific Contact Resistivity. IEEE Transactions on Electron Devices, 2010, 57, 273-281. | 3.0 | 11 |
| 68 | Interfacial Adhesion between Rough Surfaces of Polycrystalline Silicon and Its Implications for M/NEMS Technology. Journal of Adhesion Science and Technology, 2010, 24, 2545-2556. | 2.6 | 11 |
| 69 | Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. IEEE Transactions on Electron Devices, 2014, 61, 3345-3349. | 3.0 | 11 |
| 70 | Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. IEEE Transactions on Electron Devices, 2014, 61, 3296-3302. | 3.0 | 11 |
| 71 | Energy-delay performance optimization of NEM logic relay. , 2015, , . | | 11 |
| 72 | Demonstration of 50-mV Digital Integrated Circuits with Microelectromechanical Relays. , 2018, , . | | 11 |

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| 73 | Compensation of systematic variations through optimal biasing of SRAM wordlines. , 2008, , . | | 10 |
| 74 | Channel Stress and Ballistic Performance Advantages of Gate-All-Around FETs and Inserted-Oxide FinFETs. IEEE Nanotechnology Magazine, 2017, 16, 209-216. | 2.0 | 10 |
| 75 | Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications. , 2019, , . | | 10 |
| 76 | Flicker-Noise Impact on Scaling of Mixed-Signal CMOS With HfSiON. IEEE Transactions on Electron Devices, 2008, 55, 417-422. | 3.0 | 9 |
| 77 | Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method. , 2008, , . | | 9 |
| 78 | Impact of Gate-Induced Strain on MuGFET Reliability. IEEE Electron Device Letters, 2008, 29, 916-919. | 3.9 | 9 |
| 79 | DSS MOSFET With Tunable SDE Regions by Fluorine Pre-Silicidation Ion Implant. IEEE Electron Device Letters, 2010, 31, 785-787. | 3.9 | 9 |
| 80 | Recent progress and challenges for relay logic switch technology. , 2012, , . | | 8 |
| 81 | Threshold Voltage and DIBL Variability Modeling Based on Forward and Reverse Measurements for SRAM and Analog MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 1119-1126. | 3.0 | 8 |
| 82 | Tilted ion implantation as a cost-efficient sublithographic patterning technique. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2016, 34, 040608. | 1.2 | 8 |
| 83 | Impact of flash annealing on performance and reliability of high-κ/metal-gate MOSFETs for sub-45 nm CMOS. , 2007, , . | | 7 |
| 84 | Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection. IEEE Electron Device Letters, 2007, 28, 502-505. | 3.9 | 7 |
| 85 | Convex Channel Design for Improved Capacitorless DRAM Retention Time. , 2009, , . | | 7 |
| 86 | Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. IEEE Electron Device Letters, 2009, 30, 269-271. | 3.9 | 7 |
| 87 | MuGFET carrier mobility and velocity: Impacts of fin aspect ratio, orientation and stress. , 2010, , . | | 7 |
| 88 | First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. IEEE Transactions on Electron Devices, 2012, 59, 2273-2276. | 3.0 | 7 |
| 89 | NEM relay design for compact, ultra-low-power digital logic circuits. , 2014, , . | | 7 |
| 90 | Variability Study for Low-Voltage Microelectromechanical Relay Operation. IEEE Transactions on Electron Devices, 2018, 65, 1529-1534. | 3.0 | 7 |

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| 91 | Impact of random telegraph signals on V<inf>min</inf> in 45nm SRAM. , 2009, , . | | 6 |
| 92 | FinFET Design for Tolerance to Statistical Dopant Fluctuations. IEEE Nanotechnology Magazine, 2009, 8, 375-378. | 2.0 | 6 |
| 93 | Study of High-Performance Ge pMOSFET Scaling Accounting for Direct Source-to-Drain Tunneling. IEEE Transactions on Electron Devices, 2011, 58, 2895-2902. | 3.0 | 6 |
| 94 | Fabrication of $hbox{Si}_{1 - x}hbox{Ge}_{x}/hbox{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{m ON}$ and Reduced Layout-Width Dependence. IEEE Transactions on Electron Devices, 2013, 60, 153-158. | 3.0 | 6 |
| 95 | Sub-lithographic Patterning via Tilted Ion Implantation for Scaling Beyond the 7-nm Technology Node. IEEE Transactions on Electron Devices, 2017, 64, 231-236. | 3.0 | 6 |
| 96 | Effects of oxygen-inserted layers on diffusion of boron, phosphorus, and arsenic in silicon for ultra-shallow junction formation. Journal of Applied Physics, 2018, 123, . | 2.5 | 6 |
| 97 | Reducing adhesion energy of nano-electro-mechanical relay contacts by self-assembled Perfluoro (2,3-Dimethylbutan-2-ol) coating. AIP Advances, 2019, 9, 055329. | 1.3 | 6 |
| 98 | 6-T SRAM cell design with gate-all-around silicon nanowire MOSFETs. , 2013, , . | | 5 |
| 99 | Electromechanical Diode Cell Scaling for High-Density Nonvolatile Memory. IEEE Transactions on Electron Devices, 2014, 61, 1382-1387. | 3.0 | 5 |
| 100 | Tri-gate bulk MOSFET design for improved robustness to random dopant fluctuations. , 2008, , . | | 4 |
| 101 | SRAM yield enhancement with thin-BOX FD-SOI. , 2009, , . | | 4 |
| 102 | SRAM cell design considerations for SOI technology. , 2009, , . | | 4 |
| 103 | Inkjet-printed micro-electro-mechanical switches. , 2011, , . | | 4 |
| 104 | Variation Study and Implications for BJT-Based Thin-Body Capacitorless DRAM. IEEE Electron Device Letters, 2012, 33, 312-314. | 3.9 | 4 |
| 105 | Rapid melt grown germanium gate photoMOSFET on a silicon waveguide. , 2013, , . | | 4 |
| 106 | Effects of oxygen-inserted layers and oxide capping layer on dopant activation for the formation of ultrashallow p-n junctions in silicon. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2018, 36, 061211. | 1.2 | 4 |
| 107 | Simulation-Based Study of Si/Si<sub>0.9</sub>Ge<sub>0.1</sub>/Si Hetero-Channel FinFET for Enhanced Performance in Low-Power Applications. IEEE Electron Device Letters, 2019, 40, 363-366. | 3.9 | 4 |
| 108 | SRAM yield and performance enhancements with tri-gate bulk MOSFETs. , 2008, , . | | 3 |

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| 109 | Full 3D Simulation of 6T-SRAM Cells for the 22nm Node. , 2009, , . | | 3 |
| 110 | SRAM design in fully-depleted SOI technology. , 2010, , . | | 3 |
| 111 | Embedded Memory Capability of Four-Terminal Relay Technology. IEEE Transactions on Electron Devices, 2011, 58, 891-894. | 3.0 | 3 |
| 112 | Micro-relay reliability improvement by inkjet-printed microshell encapsulation. , 2013, , . | | 3 |
| 113 | Cell Ratio Tuning for High-Density SRAM Voltage Scaling With Inserted-Oxide FinFETs. IEEE Electron Device Letters, 2016, 37, 1539-1542. | 3.9 | 3 |
| 114 | Modeling Nanoelectromechanical Switches With Random Surface Roughness. IEEE Transactions on Electron Devices, 2017, 64, 2409-2416. | 3.0 | 3 |
| 115 | Simulation-Based Study of High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology. IEEE Transactions on Electron Devices, 2019, 66, 1754-1759. | 3.0 | 3 |
| 116 | Breakdown and Healing of Tungsten-Oxide Films on Microelectromechanical Relay Contacts. Journal of Microelectromechanical Systems, 2022, 31, 265-274. | 2.5 | 3 |
| 117 | Low-Standby-Power Bulk MOSFET Design Using High-$k$ Trench Isolation. IEEE Electron Device Letters, 2009, 30, 1380-1382. | 3.9 | 2 |
| 118 | Comparative Study of FinFET Versus Quasi-Planar HTI MOSFET for Ultimate Scalability. IEEE Transactions on Electron Devices, 2010, 57, 3250-3256. | 3.0 | 2 |
| 119 | Why hybridize NEMS with CMOS?. , 2014, , . | | 2 |
| 120 | Comparison of 10 nm GAA vs. FinFET 6-T SRAM performance and yield. , 2014, , . | | 2 |
| 121 | Reducing adhesion energy of micro-relay electrodes by ion beam synthesized oxide nanolayers. APL Materials, 2017, 5, 036103. | 5.1 | 2 |
| 122 | V<sub>T</sub> Adjustment by L<sub>eff</sub> Engineering for LSTP Single Gate Work-function CMOS FinFET Technology. , 2006, , . | | 1 |
| 123 | WireFET Technology for 3-D Integrated Circuits. , 2006, , . | | 1 |
| 124 | Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. IEEE Electron Device Letters, 2007, 28, 725-727. | 3.9 | 1 |
| 125 | Predictive Compact Modeling for Strain Effects in Nanoscale Transistors. , 2009, , . | | 1 |
| 126 | Electrical Characterization of Etch Rate for Micro- and Nano-Scale Gap Formation. Journal of Microelectromechanical Systems, 2010, 19, 1260-1263. | 2.5 | 1 |

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| 127 | Effectiveness of strained-Si technology for thin-body MOSFETs. , 2012, , . | | 1 |
| 128 | High-density SRAM voltage scaling enabled by inserted-oxide FinFET technology. , 2017, , . | | 1 |
| 129 | Design optimization of sub-5â€‰nm node nanosheet field effect transistors to minimize self-heating effects. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2021, 39, . | 1.2 | 1 |
| 130 | Dual-bit SONOS FinFET Non-Volatile Memory Cell and New Method of Charge Detection. , 2007, , . | | 0 |
| 131 | WetFET A Novel Fluidic Gate-Dielectric Transistor for Sensor Applications. , 2007, , . | | 0 |
| 132 | Multi-Gate MOSFETs with Dual Contact Etch Stop Liner Stressors on Tensile Metal Gate and Strained Silicon on Insulator (sSOI). , 2007, , . | | 0 |
| 133 | Steep-subthreshold-slope devices on SOI. , 2011, , . | | 0 |
| 134 | Variation-aware study of BJT-based capacitorless DRAM cell scaling limit. , 2012, , . | | 0 |
| 135 | Oxygen-inserted SegFET: A candidate for 10-nm node system-on-chip applications. , 2014, , . | | 0 |
| 136 | Tuning of Schottky barrier height using oxygen-inserted (OI) layers and fluorine implantation. AIP Advances, 2020, 10, 065310. | 1.3 | 0 |
| 137 | (Keynote) Silicon-Germanium: Enabler of Moore's Law. ECS Meeting Abstracts, 2018, , . | 0.0 | 0 |
| 138 | Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. IEEE Electron Device Letters, 2009, , . | 3.9 | 0 |