Yao-Wen Chang

List of Publications by Year
in descending order

276	5,338	186265	223800
papers	citations	28 h-index	46 g-index

280	280	280	976
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	B*-Trees. , 2000, , .		419
2	NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs With Preplaced Blocks and Density Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1228-1240.	2.7	260
3	TCG. , 2001, , .		181
4	Universal switch modules for FPGA design. ACM Transactions on Design Automation of Electronic Systems, 1996, 1, 80-101.	2.6	118
5	Modern floorplanning based on B/sup *|-tree and fast simulated annealing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 637-650.	2.7	104
6	BioRoute: A Network-Flow-Based Routing Algorithm for the Synthesis of Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1928-1941.	2.7	101
7	Placement of defect-tolerant digital microfluidic biochips using the T-tree formulation. ACM Journal on Emerging Technologies in Computing Systems, 2007, 3, 13.	2.3	86
8	Analog Placement Based on Symmetry-Island Formulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 791-804.	2.7	75
9	A Network-Flow-Based RDL Routing Algorithmz for Flip-Chip Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1417-1429.	2.7	74
10	TSV-aware analytical placement for 3D IC designs. , 2011, , .		74
11	TSV-Aware Analytical Placement for 3-D IC Designs Based on a Novel Weighted-Average Wirelength Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 497-509.	2.7	67
12	Crosstalk-driven interconnect optimization by simultaneous gate and wire sizing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2000, 19, 999-1010.	2.7	63
13	A progressive-ILP based routing algorithm for cross-referencing biochips. , 2008, , .		63
14	Modern floorplanning based on fast simulated annealing. , 2005, , .		61
15	Full-Chip Routing Considering Double-Via Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 844-857.	2.7	61
16	Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 643-653.	2.7	60
17	NTUplace4h: A Novel Routability-Driven Placement Algorithm for Hierarchical Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1914-1927.	2.7	59
18	A high-quality mixed-size analytical placer considering preplaced blocks and density constraints. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	56

#	Article	IF	Citations
19	NTUplace. , 2005, , .		55
20	Cross-Contamination Aware Design Methodology for Pin-Constrained Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 817-828.	2.7	51
21	A novel layout decomposition algorithm for triple patterning lithography. , 2012, , .		50
22	A Novel Layout Decomposition Algorithm for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 397-408.	2.7	50
23	Corner sequence - a P-admissible floorplan representation with a worst case linear-time packing scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 679-686.	3.1	48
24	TCG: A transitive closure graph-based representation for general floorplans. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 288-292.	3.1	46
25	MR: a new framework for multilevel full-chip routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 793-800.	2.7	44
26	Placement of digital microfluidic biochips using the t-tree formulation. , 2006, , .		44
27	A novel framework for multilevel routing considering routability and performance. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2002, , .	0.0	42
28	TCG-S: Orthogonal Coupling of<tex>$rm P^ast$</tex>-Admissible Representations for General Floorplans. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 968-980.	2.7	42
29	An Integer-Linear-Programming-Based Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 98-110.	2.7	42
30	Layout-Dependent Effects-Aware Analytical Analog Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1243-1254.	2.7	42
31	Routability-driven analytical placement by net overlapping removal for large-scale mixed-size designs. , 2008, , .		41
32	Flip-chip routing with unified area-I/O pad assignments for package-board co-design. , 2009, , .		41
33	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis. , 2010, , .		41
34	Temporal floorplanning using the T-tree formulation. , 0, , .		40
35	Charge-based capacitance measurement for bias-dependent capacitance. IEEE Electron Device Letters, 2006, 27, 390-392.	3.9	40
36	Efficient obstacle-avoiding rectilinear steiner tree construction. , 2007, , .		39

#	Article	IF	Citations
37	An efficient and effective analytical placer for FPGAs. , 2013, , .		39
38	Multilevel routing with antenna avoidance. , 2004, , .		38
39	High-performance global routing with fast overflow reduction. , 2009, , .		38
40	Fast Lithographic Mask Optimization Considering Process Variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1345-1357.	2.7	38
41	Crosstalk- and performance-driven multilevel full-chip routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 869-878.	2.7	37
42	MP-Trees: A Packing-Based Macro Placement Algorithm for Modern Mixed-Size Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1621-1634.	2.7	37
43	NTUplace4dr: A Detailed-Routing-Driven Placer for Mixed-Size Circuit Designs With Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 669-681.	2.7	37
44	Essential Issues in Analytical Placement Algorithms. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 145-166.	0.8	35
45	Routability-driven analytical placement for mixed-size circuit designs. , 2011, , .		33
46	Multilevel full-chip routing for the X-based architecture. , 2005, , .		32
47	Timing-driven routing for symmetrical array-based FPGAs. ACM Transactions on Design Automation of Electronic Systems, 2000, 5, 433-450.	2.6	31
48	Multilevel floorplanning/placement for large-scale modules using B*-trees. , 2003, , .		31
49	Area-I/O Flip-Chip Routing for Chip-Package Co-Design Considering Signal Skews. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 711-721.	2.7	31
50	ILP-Based Pin-Count Aware Design Methodology for Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1315-1327.	2.7	31
51	Structure-aware placement for datapath-intensive circuit designs. , 2012, , .		31
52	Generic universal switch blocks. IEEE Transactions on Computers, 2000, 49, 348-359.	3.4	29
53	Timing modeling and optimization under the transmission line model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 28-41.	3.1	29
54	Novel full-chip gridless routing considering double-via insertion. , 2006, , .		29

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55	A New Multilevel Framework for Large-Scale Interconnect-Driven Floorplanning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 286-294.	2.7	29
56	ILP-based pin-count aware design methodology for microfluidic biochips. , 2009, , .		29
57	Routability-driven placement for hierarchical mixed-size circuit designs. , 2013, , .		29
58	Simultaneous layout migration and decomposition for double patterning technology. , 2009, , .		28
59	Thermal-Driven Analog Placement Considering Device Matching. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 325-336.	2.7	26
60	Placement with symmetry constraints for analog layout design using TCG-S. , 2005, , .		25
61	Thermal-driven analog placement considering device matching. , 2009, , .		25
62	Non-uniform multilevel analog routing with matching constraints. , 2012, , .		25
63	Generic ILP-based approaches for time-multiplexed FPGA partitioning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 1266-1274.	2.7	24
64	A Novel Wire-Density-Driven Full-Chip Routing System for CMP Variation Control. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 193-206.	2.7	24
65	Pulsed-latch aware placement for timing-integrity optimization. , 2010, , .		24
66	ECO Timing Optimization Using Spare Cells and Technology Remapping. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 697-710.	2.7	24
67	Simultaneous analog placement and routing with current flow and current density considerations. , 2013, , .		24
68	Overlay-Aware Detailed Routing for Self-Aligned Double Patterning Lithography Using the Cut Process. , 2014, , .		24
69	Algorithms for an FPGA switch module routing problem with application to global routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1997, 16, 32-46.	2.7	23
70	Multiple chip planning for chip-interposer codesign. , 2013, , .		23
71	Placement with symmetry constraints for analog layout design using TCG-S. , 0, , .		22
72	Multilayer Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2007-2016.	2.7	22

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73	Global and detailed routing. , 2009, , 687-749.		22
74	Multilayer Global Routing With Via and Wire Capacity Considerations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 685-696.	2.7	22
75	Unified Analytical Global Placement for Large-Scale Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1366-1378.	2.7	21
76	Routability-Driven Blockage-Aware Macro Placement. , 2014, , .		21
77	Temporal floorplanning using the three-dimensional transitive closure subGraph. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 37.	2.6	20
78	Cross-contamination aware design methodology for pin-constrained digital microfluidic biochips. , 2010, , .		20
79	Fast timing-model independent buffered clock-tree synthesis. , 2010, , .		20
80	Nonuniform Multilevel Analog Routing With Matching Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1942-1954.	2.7	20
81	Rectilinear block placement using B*-trees. , 0, , .		19
82	Rectilinear block placement using B*-trees. ACM Transactions on Design Automation of Electronic Systems, 2003, 8, 188-202.	2.6	19
83	Efficient power/ground network analysis for power integrity-driven design methodology. , 2004, , .		19
84	Predictive formulae for OPC with applications to lithography-friendly routing. , 2008, , .		19
85	Design-hierarchy aware mixed-size placement for routability optimization. , 2010, , .		19
86	Native-Conflict and Stitch-Aware Wire Perturbation for Double Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 703-716.	2.7	19
87	Minimum-implant-area-aware detailed placement with spacing constraints. , 2016, , .		19
88	A multithreaded initial detailed routing algorithm considering global routing guides. , 2018, , .		19
89	Density gradient minimization with coupling-constrained dummy fill for CMP control. , 2010, , .		19
90	Multilevel Full-Chip Gridless Routing With Applications to Optical-Proximity Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1041-1053.	2.7	18

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91	Simultaneous Layout Migration and Decomposition for Double Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 284-294.	2.7	18
92	Simultaneous functional and timing ECO. , 2011, , .		18
93	An Integer Linear Programming Based Routing Algorithm for Flip-Chip Design. Proceedings - Design Automation Conference, 2007, , .	0.0	18
94	A novel framework for multilevel full-chip gridless routing. , 2006, , .		17
95	Power/Ground Network and Floorplan Cosynthesis for Fast Design Convergence. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 693-704.	2.7	17
96	Native-conflict-aware wire perturbation for double patterning technology. , 2010, , .		17
97	Efficient and effective packing and analytical placement for large-scale heterogeneous FPGAs. , 2014, , .		17
98	Routing-architecture-aware analytical placement for heterogeneous FPGAs. , 2015, , .		17
99	Mixed-cell-height placement with complex minimum-implant-area constraints. , 2018, , .		16
100	Double-Patterning Aware DSA Template Guided Cut Redistribution for Advanced 1-D Gridded Designs. , 2016, , .		16
101	Noise-constrained performance optimization by simultaneous gate and wire sizing based on Lagrangian relaxation. , 1999, , .		15
102	Multilevel full-chip gridless routing considering optical proximity correction. , 2005, , .		15
103	Detailed-Routing-Driven analytical standard-cell placement. , 2015, , .		15
104	Simultaneous block and I/O buffer floorplanning for flip-chip design. , 2006, , .		14
105	MP-trees. Proceedings - Design Automation Conference, 2007, , .	0.0	14
106	Simultaneous flare level and flare variation minimization with dummification in EUVL. , 2012, , .		14
107	Voltage-Island Partitioning and Floorplanning Under Timing Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 690-702.	2.7	13
108	Detailed-routability-driven analytical placement for mixed-size designs with technology and region constraints. , 2015, , .		13

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109	IMF: interconnect-driven multilevel floorplanning for large-scale building-module designs. , 0, , .		12
110	Metal-Density-Driven Placement for CMP Variation and Routability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2145-2155.	2.7	12
111	Recent research development in flip-chip routing. , 2010, , .		12
112	Predictive Formulae for OPC With Applications to Lithography-Friendly Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 40-50.	2.7	12
113	Fast Timing-Model Independent Buffered Clock-Tree Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1393-1404.	2.7	12
114	EUV and e-beam manufacturability. , 2015, , .		12
115	Layout-dependent-effects-aware analytical analog placement. , 2015, , .		12
116	Redistribution layer routing for integrated fan-out wafer-level chip-scale packages. , 2016, , .		12
117	Circular-contour-based obstacle-aware macro placement. , 2016, , .		12
118	Mixed-cell-height legalization considering technology and region constraints. , 2018, , .		12
119	An exact jumper insertion algorithm for antenna effect avoidance/fixing. , 2005, , .		11
120	SoC test scheduling using the B-tree based floorplanning technique. , 2005, , .		11
121	An optimal jumper insertion algorithm for antenna avoidance/fixing on general routing trees with obstacles. , 2006, , .		11
122	TRECO: Dynamic technology remapping for timing Engineering Change Orders. , 2010, , .		11
123	High variation-tolerant obstacle-avoiding clock mesh synthesis with symmetrical driving trees. , 2010, , .		11
124	TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1723-1733.	2.7	11
125	Timing ECO Optimization Via BÃ©zier Curve Smoothing and Fixability Identification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1857-1866.	2.7	11
126	Nanowire-aware routing considering high cut mask complexity. , 2015, , .		11

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127	A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 533-546.	2.7	11
128	Arbitrarily shaped rectilinear module placement using the transitive closure graph representation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 886-901.	3.1	10
129	Voltage Island Aware Floorplanning for Power and Timing Optimization. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	10
130	Recent Research and Emerging Challenges in Physical Design for Manufacturability/Reliability. , 2007, , .		10
131	Multilevel Full-Chip Routing With Testability and Yield Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1625-1636.	2.7	10
132	Redundant-wires-aware ECO timing and mask cost optimization. , 2010, , .		10
133	An Efficient Pre-Assignment Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 878-889.	2.7	10
134	Escape Routing for Staggered-Pin-Array PCBs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1347-1356.	2.7	10
135	Coupling-Aware Length-Ratio-Matching Routing for Capacitor Arrays in Analog Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 161-172.	2.7	10
136	Cut redistribution with directed self-assembly templates for advanced 1-D gridded layouts. , 2016, , .		10
137	Mixed-cell-height placement considering drain-to-drain abutment. , 2018, , .		10
138	Analytical solution of Poisson's equation and its application to VLSI global placement. , 2018, , .		10
139	Post-floorplanning power/ground ring synthesis for multiple-supply-voltage designs. , 2009, , .		9
140	QB-trees. , 2016, , .		9
141	Mixed-Cell-Height Detailed Placement Considering Complex Minimum-Implant-Area Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2128-2141.	2.7	9
142	Mixed-Cell-Height Legalization Considering Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5128-5141.	2.7	9
143	Timing-driven routing for symmetrical-array-based FPGAs. , 0, , .		8
144	Simultaneous Floorplan and Buffer-Block Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 694-703.	2.7	8

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145	An Optimal Jumper-Insertion Algorithm for Antenna Avoidance/Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1818-1829.	2.7	8
146	An Optimal Network-Flow-Based Simultaneous Diode and Jumper Insertion Algorithm for Antenna Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1055-1065.	2.7	8
147	Routing for manufacturability and reliability. IEEE Circuits and Systems Magazine, 2009, 9, 20-31.	2.3	8
148	A corner stitching compliant B[∗]-tree representation and its applications to analog placement. , 2011, , .		8
149	Graph-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 189-201.	2.7	8
150	A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing. , 2019, , .		8
151	A clustering- and probability-based approach for time-multiplexed FPGA partitioning. , 0, , .		7
152	Crosstalk-constrained performance optimization by using wire sizing and perturbation. , 0, , .		7
153	Matching-based algorithm for FPGA channel segmentation design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 784-791.	2.7	7
154	Comment on "Generic universal switch blocks". IEEE Transactions on Computers, 2002, 51, 93-95.	3.4	7
155	Placement with alignment and performance constraints using the B*-tree representation-. , 0, , .		7
156	Delay modeling for buffered RLY/RLC trees. , 0, , .		7
157	A Progressive-ILP-Based Routing Algorithm for the Synthesis of Cross-Referencing Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1295-1306.	2.7	7
158	Escape routing for staggered-pin-array PCBs. , 2011, , .		7
159	Coupling-aware length-ratio-matching routing for capacitor arrays in analog integrated circuits. , 2013, , .		7
160	Stitch-aware routing for multiple e-beam lithography. , 2013, , .		7
161	Double patterning lithography-aware analog placement. , 2013, , .		7
162	Fast lithographic mask optimization considering process variation. , 2014, , .		7

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163	Obstacle-Avoiding Free-Assignment Routing for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 224-236.	2.7	7
164	A New Asynchronous Pipeline Template for Power and Performance Optimization. , 2014, , .		7
165	Fogging Effect Aware Placement in Electron Beam Lithography. , 2017, , .		7
166	Novel proximal group ADMM for placement considering fogging and proximity effects. , 2018, , .		7
167	Graph matching-based algorithms for FPGA segmentation design. , 1998, , .		6
168	Quasi-universal switch matrices for FPD design. IEEE Transactions on Computers, 1999, 48, 1107-1122.	3.4	6
169	A High-Quality Mixed-Size Analytical Placer Considering Preplaced Blocks and Density Constraints. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
170	Post-placement leakage optimization for partially dynamically reconfigurable FPGAs. , 2007, , .		6
171	Metal-density driven placement for cmp variation and routability. , 2008, , .		6
172	T-trees. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-28.	2.6	6
173	A SAT-based routing algorithm for cross-referencing biochips. , 2011, , .		6
174	Overlay-Aware Detailed Routing for Self-Aligned Double Patterning Lithography Using the Cut Process. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1519-1531.	2.7	6
175	Generalized augmented lagrangian and its applications to VLSI global placement. , 2018, , .		6
176	BiG. , 2019, , .		6
177	MDP-trees. , 2019, , .		6
178	Inductance Modeling for On-Chip Interconnects. Analog Integrated Circuits and Signal Processing, 2003, 35, 65-78.	1.4	5
179	Noise-aware buffer planning for interconnect-driven floorplanning. , 2003, , .		5
180	A routing algorithm for flip-chip design. , 0, , .		5

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181	Multilevel full-chip gridless routing considering optical proximity correction. , 0, , .		5
182	Multilevel routing with jumper insertion for antenna avoidance. The Integration VLSI Journal, 2006, 39, 420-432.	2.1	5
183	Novel full-chip gridless routing considering double-via insertion. Proceedings - Design Automation Conference, 2006, , .	0.0	5
184	Challenges and Solutions in Modern VLSI Placement. , 2007, , .		5
185	An Exact Jumper-Insertion Algorithm for Antenna Violation Avoidance/Fixing Considering Routing Obstacles. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 719-733.	2.7	5
186	ECO timing optimization using spare cells. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	5
187	Area-I/O flip-chip routing for chip-package co-design. , 2008, , .		5
188	Floorplanning. , 2009, , 575-634.		5
189	A chip-package-board co-design methodology. , 2012, , .		5
190	Stitch-Aware Routing for Multiple E-Beam Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 471-482.	2.7	5
191	Non-stitch triple patterning-aware routing based on conflict graph pre-coloring. , 2015, , .		5
192	Timing-driven cell placement optimization for early slack histogram compression. , 2016, , .		5
193	Simultaneous EUV Flare Variation Minimization and CMP Control by Coupling-Aware Dummification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 598-610.	2.7	5
194	Graph-Based Logic Bit Slicing for Datapath-Aware Placement. , 2017, , .		5
195	WB-trees. , 2018, , .		5
196	Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs. , 2009, , .		5
197	Novel wire density driven full-chip routing for CMP variation control. , 2007, , .		4
198	Unified analytical global placement for large-scale mixed-size circuit designs. , 2010, , .		4

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199	PRICE: Power reduction by placement and clock-network co-synthesis for pulsed-latch designs. , 2011, , .		4
200	Voltage-Drop Aware Analytical Placement by Global Power Spreading for Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1649-1662.	2.7	4
201	Timing ECO optimization using metal-configurable gate-array spare cells. , 2012, , .		4
202	Obstacle-avoiding free-assignment routing for flip-chip designs. , 2012, , .		4
203	Simultaneous EUV Flare Variation Minimization and CMP Control with Coupling-Aware Dummification. , 2014, , .		4
204	Simultaneous EUV flare- and CMP-aware placement. , 2014, , .		4
205	Layout decomposition for Spacer-is-Metal (SIM) self-aligned double patterning. , 2015, , .		4
206	DSA-compliant routing for two-dimensional patterns using block copolymer lithography. , 2016, , .		4
207	VCR. , 2016, , .		4
208	Efficient multi-layer obstacle-avoiding region-to-region rectilinear steiner tree construction. , 2018, , .		4
209	Analytical Placement Considering the Electron-Beam Fogging Effect. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 560-573.	2.7	4
210	Simultaneous Buffer-sizing and Wire-sizing for Clock Trees Based on Lagrangian Relaxation. VLSI Design, 2002, 15, 587-594.	0.5	4
211	VLSI Structure-aware Placement for Convolutional Neural Network Accelerator Units. , 2021, , .		4
212	High-Correlation 3D Routability Estimation for Congestion-guided Global Routing. , 2022, , .		4
213	Analysis of FPGA/FPIC switch modules. ACM Transactions on Design Automation of Electronic Systems, 2003, 8, 11-37.	2.6	3
214	RLC Coupling-Aware Simulation for On-Chip Buses and their Encoding for Delay Reduction. , 0, , .		3
215	Statistical circuit optimization considering device andinterconnect process variations. , 2007, , .		3
216	Efficient multi-layer obstacle-avoiding rectilinear steiner tree construction. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3

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