Mathias Soeken

List of Publications by Year
in descending order

91	1,652	471509 17	552781 26
papers	citations	h-index	g-index

93	93	93	655
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Xor-And-Inverter Graphs for Quantum Compilation. Npj Quantum Information, 2022, 8, .	6.7	7
2	Lowering the T-depth of Quantum Circuits via Logic Network Optimization. ACM Transactions on Quantum Computing, 2022, 3, 1-15.	4.3	2
3	Three-Input Gates for Logic Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2184-2188.	2.7	9
4	SAT-Based Exact Synthesis: Encodings, Topology Families, and Parallelism. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 871-884.	2.7	23
5	Advanced Functional Decomposition Using Majority and Its Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1621-1634.	2.7	12
6	Extending Boolean Methods for Scalable Logic Synthesis. IEEE Access, 2020, 8, 226828-226844.	4.2	4
7	LUT-Based Hierarchical Reversible Logic Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1675-1688.	2.7	24
8	Scalable Generic Logic Synthesis. , 2019, , .		20
9	Reversible Pebble Games for Reducing Qubits in Hierarchical Quantum Circuit Synthesis. , 2019, , .		3
10	Structural rewriting in XOR-majority graphs. , 2019, , .		17
11	Mapping Monotone Boolean Functions into Majority. IEEE Transactions on Computers, 2019, 68, 791-797.	3.4	5
12	Logic Synthesis for Established and Emerging Computing. Proceedings of the IEEE, 2019, 107, 165-184.	21.3	24
13	On-the-fly and DAG-aware: Rewriting Boolean Networks with Exact Synthesis. , 2019, , .		26
14	Logic Synthesis for RRAM-Based In-Memory Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1422-1435.	2.7	37
15	SAT based exact synthesis using DAG topology families. , 2018, , .		7
16	Majority logic synthesis. , 2018, , .		10
17	The complexity of error metrics. Information Processing Letters, 2018, 139, 1-7.	0.6	6
18	Practical exact synthesis. , 2018, , .		15

#	Article	IF	Citations
19	Pairs of majority-decomposing functions. Information Processing Letters, 2018, 139, 35-38.	0.6	1
20	metaSMT: focus on your application and not on solver integration. International Journal on Software Tools for Technology Transfer, 2017, 19, 605-621.	1.9	7
21	Exact Synthesis of Majority-Inverter Graphs and Its Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1842-1855.	2.7	62
22	Hierarchical Reversible Logic Synthesis Using LUTs. , 2017, , .		16
23	Design automation and design space exploration for quantum computers. , 2017, , .		21
24	Enabling exact delay synthesis. , 2017, , .		9
25	Multilevel design understanding. , 2016, , .		5
26	An MIG-based compiler for programmable logic-in-memory architectures. , 2016, , .		30
27	Technology Mapping of Reversible Circuits to Clifford+T Quantum Circuits. , 2016, , .		28
28	Unlocking efficiency and scalability of reversible logic synthesis using conventional logic synthesis. , 2016, , .		19
29	Verifying the structure and behavior in UML/OCL models using satisfiability solvers. IET Cyber-Physical Systems: Theory and Applications, 2016, 1, 49-59.	3.3	16
30	Multi-objective BDD optimization for RRAM based circuit design. , 2016, , .		15
31	SyReC: A hardware description language for the specification and synthesis of reversible circuits. The Integration VLSI Journal, 2016, 53, 39-53.	2.1	20
32	Complexity of reversible circuits and their quantum implementations. Theoretical Computer Science, 2016, 618, 85-106.	0.9	17
33	BDD minimization for approximate computing. , 2016, , .		41
34	Embedding of Large Boolean Functions for Reversible Logic. ACM Journal on Emerging Technologies in Computing Systems, 2016, 12, 1-26.	2.3	34
35	Enumeration of Reversible Functions and Its Application to Circuit Complexity. Lecture Notes in Computer Science, 2016, , 255-270.	1.3	10
36	A Fast Symbolic Transformation Based Algorithm for Reversible Logic Synthesis. Lecture Notes in Computer Science, 2016, , 307-321.	1.3	14

#	Article	IF	Citations
37	Formal Verification of Integer Multipliers by Combining GrÃ¶bner Basis with Logic Reduction. , 2016, , .		49
38	Optimizing Majority-Inverter Graphs With Functional Hashing. , 2016, , .		19
39	Simulation graphs for reverse engineering. , 2015, , .		9
40	Reversible circuit rewriting with simulated annealing. , 2015, , .		12
41	Multi-Objective BDD Optimization with Evolutionary Algorithms. , 2015, , .		8
42	Specification-driven model transformation testing. Software and Systems Modeling, 2015, 14, 623-644.	2.7	32
43	Verification of Static Aspects. , 2015, , 57-108.		0
44	Verification of Dynamic Aspects. , 2015, , 109-129.		0
45	Ricercar: A Language for Describing andÂRewriting Reversible Circuits with Ancillae and Its Permutation Semantics. Lecture Notes in Computer Science, 2015, , 200-215.	1.3	3
46	MetaSMT: a unified interface to SMT-LIB2. , 2014, , .		1
47	Automated and quality-driven requirements engineering. , 2014, , .		6
48	Automating the translation of assertions using natural language processing techniques. , 2014, , .		12
49	Self-Verification as the Key Technology for Next Generation Electronic Systems. , 2014, , .		9
50	Trading off circuit lines and gate costs in the synthesis of reversible logic. The Integration VLSI Journal, 2014, 47, 284-294.	2.1	46
51	Quantum Circuit Optimization by Hadamard Gate Reduction. Lecture Notes in Computer Science, 2014, , 149-162.	1.3	19
52	Mapping NCV Circuits to Optimized Clifford+T Circuits. Lecture Notes in Computer Science, 2014, , 163-175.	1.3	35
53	Behaviour Driven Development for Tests and Verification. Lecture Notes in Computer Science, 2014, , 61-77.	1.3	5
54	Requirements Engineering for Cyber-Physical Systems. Lecture Notes in Computer Science, 2014, , 281-288.	1.3	15

#	Article	IF	Citations
55	Formal Specification Level. Lecture Notes in Electrical Engineering, 2014, , 37-52.	0.4	4
56	Quantum circuits employing roots of the Pauli matrices. Physical Review A, 2013, 88, .	2.5	35
57	Grammar-based program generation based on model finding. , 2013, , .		1
58	Debugging of Reversible Circuits Using pDDs. , 2013, , .		2
59	Improving the mapping of reversible circuits to quantum circuits using multiple target lines. , 2013, , .		50
60	Determining Relevant Model Elements for the Verification of UML/OCL Specifications. , 2013, , .		6
61	Exact Template Matching Using Boolean Satisfiability. , 2013, , .		17
62	Towards a Generic Verification Methodology for System Models. , 2013, , .		7
63	Lips: An IDE for model driven engineering based on natural language processing. , 2013, , .		11
64	Towards automatic scenario generation from coverage information. , 2013, , .		1
65	Hardware-Software Co-Visualization: Developing systems in the holodeck. , 2013, , .		3
66	Using Ï€DDs in the Design of Reversible Circuits. Lecture Notes in Computer Science, 2013, , 197-203.	1.3	1
67	White Dots do Matter: Rewriting Reversible Logic Circuits. Lecture Notes in Computer Science, 2013, , 196-208.	1.3	27
68	Reducing the Depth of Quantum Circuits Using Additional Circuit Lines. Lecture Notes in Computer Science, 2013, , 221-233.	1.3	18
69	Property Checking of Quantum Circuits Using Quantum Multiple-Valued Decision Diagrams. Lecture Notes in Computer Science, 2013, , 183-196.	1.3	4
70	Debugging of inconsistent UML/OCL models. , 2012, , .		21
71	A Synthesis Flow for Sequential Reversible Circuits. , 2012, , .		11
72	Eliminating invariants in UML/OCL models. , 2012, , .		3

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73	Synthesis of reversible circuits with minimal lines for large functions. , 2012, , .		84
74	Circuit Line Minimization in the HDL-Based Synthesis of Reversible Logic. , 2012, , .		11
75	Behavior Driven Development for circuit design and verification. , 2012, , .		12
76	Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines. , 2012, , .		22
77	Optimizing the Mapping of Reversible Circuits to Four-Valued Quantum Gate Circuits. , 2012, , .		20
78	RevKit: An Open Source Toolkit for the Design of Reversible Circuits. Lecture Notes in Computer Science, 2012, , 64-76.	1.3	51
79	Assisted Behavior Driven Development Using Natural Language Processing. Lecture Notes in Computer Science, 2012, , 269-287.	1.3	55
80	Completeness-Driven Development. Lecture Notes in Computer Science, 2012, , 38-50.	1.3	12
81	Automatic property generation for the formal verification of bus bridges. , 2011, , .		2
82	Towards automatic determination of problem bounds for object instantiation in static model verification. , 2011, , .		5
83	Designing a RISC CPU in Reversible Logic. , 2011, , .		7
84	Verifying dynamic aspects of UML models. , 2011, , .		44
85	Encoding OCL Data Types for SAT-Based Verification of UML/OCL Models. Lecture Notes in Computer Science, 2011, , 152-170.	1.3	29
86	Reducing the number of lines in reversible circuits. , 2010, , .		49
87	Verifying UML/OCL models using Boolean satisfiability. , 2010, , .		72
88	Hierarchical synthesis of reversible circuits using positive and negative Davio decomposition. , 2010, , .		25
89	Window optimization of reversible and quantum circuits. , 2010, , .		26
90	Using Higher Levels of Abstraction for Solving Optimization Problems by Boolean Satisfiability. , 2008, , .		4

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91	ROS: Resource-constrained Oracle Synthesis for Quantum Computers. Electronic Proceedings in Theoretical Computer Science, EPTCS, 0, 318, 119-130.	0.8	3