List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/2440368/publications.pdf Version: 2024-02-01

		5876	3997
412	35,760	81	176
papers	citations	h-index	g-index
417	417	417	22115
all docs	docs citations	times ranked	citing authors

#	Article	IF	CITATIONS
1	Electro-Thermal Confinement Enables Improved Superlattice Phase Change Memory. IEEE Electron Device Letters, 2022, 43, 204-207.	2.2	11
2	Bandgap Extraction at 10 K to Enable Leakage Control in Carbon Nanotube MOSFETs. IEEE Electron Device Letters, 2022, 43, 490-493.	2.2	11
3	CeO ₂ Doping of Hf _{0.5} Zr _{0.5} O ₂ Thin Films for High Endurance Ferroelectric Memories. Advanced Electronic Materials, 2022, 8, .	2.6	5
4	Laser-induced patterning for a diffraction grating using the phase change material of Ge ₂ Sb ₂ Te ₅ (GST) as a spatial light modulator in X-ray optics: a proof of concept. Optical Materials Express, 2022, 12, 1408.	1.6	2
5	Impact of Metal Hybridization on Contact Resistance and Leakage Current of Carbon Nanotube Transistors. IEEE Electron Device Letters, 2022, 43, 1367-1370.	2.2	5
6	SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge. IEEE Transactions on Electron Devices, 2021, 68, 6637-6643.	1.6	34
7	Intracellular detection and communication of a wireless chip in cell. Scientific Reports, 2021, 11, 5967.	1.6	10
8	Electrical tuning of phase-change antennas and metasurfaces. Nature Nanotechnology, 2021, 16, 667-672.	15.6	196
9	Ultrathin Three-Monolayer Tunneling Memory Selectors. ACS Nano, 2021, 15, 8484-8491.	7.3	8
10	Toward Low-Temperature Solid-Source Synthesis of Monolayer MoS ₂ . ACS Applied Materials & Interfaces, 2021, 13, 41866-41874.	4.0	21
11	Application-driven synthesis and characterization of hexagonal boron nitride deposited on metals and carbon nanotubes. 2D Materials, 2021, 8, 045024.	2.0	2
12	Ultralow–switching current density multilevel phase-change memory on a flexible substrate. Science, 2021, 373, 1243-1247.	6.0	78
13	RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays. IEEE Transactions on Electron Devices, 2021, 68, 4397-4403.	1.6	24
14	Illusion of large on-chip memory by networked computing chips for neural network inference. Nature Electronics, 2021, 4, 71-80.	13.1	15
15	Layered Semiconducting 2D Materials for Future Transistor Applications. Small Structures, 2021, 2, 2000103.	6.9	85
16	Reduced HfOâ,, Resistive Memory Variability by Inserting a Thin SnOâ,, as Oxygen Stopping Layer. IEEE Electron Device Letters, 2021, 42, 1778-1781.	2.2	4
17	Self-assembly for electronics. MRS Bulletin, 2020, 45, 807-814.	1.7	10
18	Design Space Analysis for Cross-Point 1S1MTJ MRAM: Selector–MTJ Cooptimization. IEEE Transactions on Electron Devices, 2020, 67, 3102-3108.	1.6	3

#	Article	IF	CITATIONS
19	Molybdenum oxide on carbon nanotube: Doping stability and correlation with work function. Journal of Applied Physics, 2020, 128, 045111.	1.1	6
20	Two-Fold Reduction of Switching Current Density in Phase Change Memory Using Biâ,,Teâ,ƒ Thermoelectric Interfacial Layer. IEEE Electron Device Letters, 2020, 41, 1657-1660.	2.2	17
21	Bidirectional Analog Conductance Modulation for RRAM-Based Neural Networks. IEEE Transactions on Electron Devices, 2020, 67, 4904-4910.	1.6	4
22	Wafer-scale single-crystal hexagonal boron nitride monolayers on CuÂ(111). Nature, 2020, 579, 219-223.	13.7	409
23	Hyperdimensional computing nanosystem: in-memory computing using monolithic 3D integration of RRAM and CNFET. , 2020, , 195-219.		2
24	A Density Metric for Semiconductor Technology [Point of View]. Proceedings of the IEEE, 2020, 108, 478-482.	16.4	25
25	Heterogeneous 3D Nano-systems: The N3XT Approach?. The Frontiers Collection, 2020, , 127-151.	0.1	6
26	Beyond-Silicon Devices: Considerations for Circuits and Architectures. , 2019, , 1-19.		0
27	Localized Triggering of the Insulator-Metal Transition in VO ₂ Using a Single Carbon Nanotube. ACS Nano, 2019, 13, 11070-11077.	7.3	25
28	Fast Spiking of a Mott VO ₂ –Carbon Nanotube Composite Device. Nano Letters, 2019, 19, 6751-6755.	4.5	56
29	Optoelectronic resistive random access memory for neuromorphic vision sensors. Nature Nanotechnology, 2019, 14, 776-782.	15.6	783
30	Demonstration of 40-nm Channel Length Top-Gate p-MOSFET of WS ₂ Channel Directly Grown on SiO\$_{{x}}\$ /Si Substrates Using Area-Selective CVD Technology. IEEE Transactions on Electron Devices, 2019, 66, 5381-5386.	1.6	5
31	How 2D semiconductors could extend Moore's law. Nature, 2019, 567, 169-170.	13.7	222
32	Gate Quantum Capacitance Effects in Nanoscale Transistors. Nano Letters, 2019, 19, 7130-7137.	4.5	6
33	Graphene and two-dimensional materials for silicon technology. Nature, 2019, 573, 507-518.	13.7	936
34	Low-Temperature Side Contact to Carbon Nanotube Transistors: Resistance Distributions Down to 10 nm Contact Length. Nano Letters, 2019, 19, 1083-1089.	4.5	42
35	Intrinsic limits of leakage current in self-heating-triggered threshold switches. Applied Physics Letters, 2019, 114, .	1.5	9
36	Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. Nature Communications, 2019, 10, 2161.	5.8	141

#	Article	IF	CITATIONS
37	Understanding the switching mechanism of interfacial phase change memory. Journal of Applied Physics, 2019, 125, .	1.1	35
38	A Physics-Based Compact Model for CBRAM Retention Behaviors Based on Atom Transport Dynamics and Percolation Theory. IEEE Electron Device Letters, 2019, 40, 647-650.	2.2	13
39	Engineering thermal and electrical interface properties of phase change memory with monolayer MoS2. Applied Physics Letters, 2019, 114, .	1.5	36
40	Scanning microwave imaging of optically patterned Ge2Sb2Te5. Applied Physics Letters, 2019, 114, 093106.	1.5	3
41	Ternary content-addressable memory with MoS2 transistors for massively parallel data search. Nature Electronics, 2019, 2, 108-114.	13.1	83
42	<i>In-Situ</i> Grown Graphene Enabled Copper Interconnects With Improved Electromigration Reliability. IEEE Electron Device Letters, 2019, 40, 815-817.	2.2	24
43	Vertical Sidewall MoS ₂ Growth and Transistors. , 2019, , .		2
44	Monolithic 3-D Integration. IEEE Micro, 2019, 39, 16-27.	1.8	24
45	Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)—Part I: Accurate and Computationally Efficient Modeling. IEEE Transactions on Electron Devices, 2019, 66, 5139-5146.	1.6	18
46	Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)—Part II: Design Guidelines for Device, Array, and Architecture. IEEE Transactions on Electron Devices, 2019, 66, 5147-5154.	1.6	22
47	The N3XT Approach to Energy-Efficient Abundant-Data Computing. Proceedings of the IEEE, 2019, 107, 19-48.	16.4	71
48	Spatial Separation of Carrier Spin by the Valley Hall Effect in Monolayer WSe ₂ Transistors. Nano Letters, 2019, 19, 770-774.	4.5	31
49	Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell. IEEE Transactions on Electron Devices, 2019, 66, 641-646.	1.6	43
50	Device and materials requirements for neuromorphic computing. Journal Physics D: Applied Physics, 2019, 52, 113001.	1.3	105
51	Recommended Methods to Study Resistive Switching Devices. Advanced Electronic Materials, 2019, 5, 1800143.	2.6	452
52	Neuro-inspired computing with emerging memories: where device physics meets learning algorithms. , 2019, , .		2
53	Carbon nanomaterials for non-volatile memories. Nature Reviews Materials, 2018, 3, .	23.3	87
54	Scaling the CBRAM Switching Layer Diameter to 30 nm Improves Cycling Endurance. IEEE Electron Device Letters, 2018, 39, 23-26.	2.2	24

55Unipole n Type Black Phosphones Transistors with Low Work Function Contacts. Nano Letters, 2018,1.54.066Effect of thermal insulation on the electrical characteristics of NbOx threshold switches. Applied1.52667Brain-hapked computing exploring carbon nanotube FFTs and resistive RAM. Hyperdimensional8468Photoelectrochemical Water Oxidation by Gaks Nanowire Arrays Protected with Atomic Layer1.0669Frist Principles Study of Memory Selectors using Heteroplanctions of 2D Layered Materials, 2018, 17, 952-937.260Artificial optic neural synapse for colored and color-mixed pattern recognition. Nature5.849261Hyperdimensional Computing Exploring Carbon Nanotube FFTS, Resistive RAM, and Their Monolithic 3D3.549262Visite EEE Name of Solid State Circuits, 2018, 53, 3183 3196.1.18763Selector Requirements for Ters/Bit Ultra-High-Density 3D Vertical RRAM, 2018,1.52.764Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback1.52.765Coming Up N3XT, After 2D Scaling of SI CMOS., 2018,2.018, 1, 458-465.1.5.14.566Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465.1.13.53.567Energy Efficient Phase Change Memory Programming by Nanosecond Pulses, 2018, 1, 333-343.1.13.5168Internalization of subcellular-scale microfibricated chips by healthy and cancer cells. PLoS ONE,1.13.5169Internalization of subcel	#	Article	IF	CITATIONS
56 Physics Letters, 2018, 112, . 1.5 26 57 Brain-inspired computing exploiting carbon nanotube FETs and resistive RAM: Hyperdimensional computing case study., 2018, . 84 58 Photoelectrochemical Water Oxidation by GaAs Nanowire Arrays Protected with Atomic Layer Deposited NiO x Electrocatalysts. Journal of Electronic Materials, 2018, 47, 932-937. 1.0 6 59 First Principles Study of Memory Selectors using Heterglunctions of 2D Layered Materials., 2018, 2 60 Artificial optic-neural synapse for colored and color-mixed pattern recognition. Nature Communications, 2018, 9, 5106. 3.8 462 61 Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.3 49 62 Understanding Energy Efficiency Benefits of Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, 11 87 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback 1.5 27 65 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, 7 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 <td< td=""><td>55</td><td></td><td>4.5</td><td>40</td></td<>	55		4.5	40
57 computing case study, 2015,	56		1.5	26
38 Deposited NIO x Electrocatalysts, Journal of Electronic Materials, 2018, 47, 932-937. 1.0 6 39 First Principles Study of Memory Selectors using Heterojunctions of 2D Layered Materials., 2018, 2 60 Artificial optic-neural synapse for colored and color-mixed pattern recognition. Nature 5.8 462 61 Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 62 Understanding Energy Efficiency Benefits of Carbon Nanotube FIeld-Effect Transistors for Digital 1.1 87 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, 11 87 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback 1.5 27 65 Coming Up N3XT, After 2D Scaling of SI CMOS., 2018, 7 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 459 67 Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018, 3 3 68 Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 1.1 5 69 In-memory computing with resistive switching devices. Nature Electronics	57			84
60 Artificial optic-neural synapse for colored and color-mixed pattern recognition. Nature 5.8 462 61 Hyperdimensional Computing Exploring Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 62 Understanding Energy Efficiency Benefits of Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 63 Selector Requirements of Solid State Circuits, 2018, 53, 3183-3196. 1.1 87 64 Inderstanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital 1.1 87 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, 11 11 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism. Applied Physics Letters, 2018, 112, 7 65 Coming Up N3XT, After 2D Scaling of SI CMOS., 2018, 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 459 67 Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018, 3 3 68 Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 1.1 5 69 In-memory computing with resistiv	58		1.0	6
60 Communications, 2018, 9, 5106. 5.8 462 61 Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 61 Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D 3.5 49 62 Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital 1.1 87 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, 11 11 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism. Applied Physics Letters, 2018, 112, 7 65 Coming Up N3XT, After 2D Scaling of Si CMOS., 2018, 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 459 67 Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses, 2018, 3 3 68 Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712. 1.1 5 69 In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343. 13.1 1,316	59	First Principles Study of Memory Selectors using Heterojunctions of 2D Layered Materials. , 2018, , .		2
11 Integration. IEEE Journal of Solid-State Circuits, 2018, 53, 3183-3196. 3.5 49 62 Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital 1.1 87 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, ,. 11 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback 1.5 27 65 Coming Up N3XT, After 2D Scaling of Si CMOS., 2018, ,. 7 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 459 67 Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018, 3 3 68 Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 1.1 5 69 In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343. 13.1 1,316	60	Artificial optic-neural synapse for colored and color-mixed pattern recognition. Nature Communications, 2018, 9, 5106.	5.8	462
62 VLSI. IEEE Nanotechnology Magazine, 2018, 17, 1259-1269. 1.1 87 63 Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM., 2018, , . 11 64 Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism. Applied Physics Letters, 2018, 112, . 1.5 27 65 Coming Up N3XT, After 2D Scaling of Si CMOS., 2018, , . 7 7 66 Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465. 13.1 459 67 Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018, 3 3 68 Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712. 13.1 4,51 69 In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343. 13.1 1,316	61		3.5	49
64Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism. Applied Physics Letters, 2018, 112,.1.52765Coming Up N3XT, After 2D Scaling of Si CMOS., 2018,.766Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465.13.145967Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018,.368Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712.1.1569In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.13.11,316	62		1.1	87
64mechanism. Applied Physics Letters, 2018, 112,	63	Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM. , 2018, , .		11
66Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465.13.145967Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses., 2018, ,.368Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712.1.1569In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.13.11,316	64		1.5	27
67Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses. , 2018, , .368Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712.1.1569In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.13.11,316	65	Coming Up N3XT, After 2D Scaling of Si CMOS. , 2018, , .		7
68Internalization of subcellular-scale microfabricated chips by healthy and cancer cells. PLoS ONE, 2018, 13, e0194712.1.1569In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.13.11,316	66	Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465.	13.1	459
68 2018, 13, e0194712. 1.1 5 69 In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343. 13.1 1,316	67	Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses. , 2018, , .		3
	68		1.1	5
70Face classification using electronic synapses. Nature Communications, 2017, 8, 15199.5.8683	69	In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.	13.1	1,316
	70	Face classification using electronic synapses. Nature Communications, 2017, 8, 15199.	5.8	683
71 Hysteresis-Free Carbon Nanotube Field-Effect Transistors. ACS Nano, 2017, 11, 4785-4791. 7.3 50	71	Hysteresis-Free Carbon Nanotube Field-Effect Transistors. ACS Nano, 2017, 11, 4785-4791.	7.3	50

72 Synaptic Devices Based on Phase-Change Memory. , 2017, , 19-51.

#	Article	IF	CITATIONS
73	Resistive RAM-Centric Computing: Design and Modeling Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2263-2273.	3.5	61
74	Universal Selective Dispersion of Semiconducting Carbon Nanotubes from Commercial Sources Using a Supramolecular Polymer. ACS Nano, 2017, 11, 5660-5669.	7.3	47
75	Ultrafast Accelerated Retention Test Methodology for RRAM Using Micro Thermal Stage. IEEE Electron Device Letters, 2017, 38, 863-866.	2.2	7
76	Statistical study of RRAM MLC SET variability induced by filament morphology. , 2017, , .		1
77	The End of Moore's Law: A New Beginning for Information Technology. Computing in Science and Engineering, 2017, 19, 41-50.	1.2	481
78	Real-Time Observation of the Electrode-Size-Dependent Evolution Dynamics of the Conducting Filaments in a SiO ₂ Layer. ACS Nano, 2017, 11, 4097-4104.	7.3	79
79	Phase-Change Memory—Towards a Storage-Class Memory. IEEE Transactions on Electron Devices, 2017, 64, 4374-4385.	1.6	291
80	3D nanosystems enable embedded abundant-data computing. , 2017, , .		6
81	A simple technique to design microfluidic devices for system integration. Analytical Methods, 2017, 9, 6349-6356.	1.3	2
82	AC stress and electronic effects on SET switching of HfO2 RRAM. Applied Physics Letters, 2017, 111, 093502.	1.5	1
83	Dual-Layer Dielectric Stack for Thermally-Isolated Low-Power Phase-Change Memory. , 2017, , .		5
84	Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature, 2017, 547, 74-78.	13.7	577
85	Resistive random access memory (RRAM) technology: From material, device, selector, 3D integration to bottom-up fabrication. Journal of Electroceramics, 2017, 39, 21-38.	0.8	79
86	Carbon Nanotubes for Monolithic 3D ICs. , 2017, , 315-333.		2
87	Device and Circuit Interaction Analysis of Stochastic Behaviors in Cross-Point RRAM Arrays. IEEE Transactions on Electron Devices, 2017, 64, 4928-4936.	1.6	22
88	Dual-Layer Dielectric Stack for Thermally Isolated Low-Energy Phase-Change Memory. IEEE Transactions on Electron Devices, 2017, 64, 4496-4502.	1.6	29
89	Challenges and opportunities toward online training acceleration using RRAM-based hardware neural network. , 2017, , .		26
90	Sub-15 nm nanowires enabled by cryo pulsed self-aligned nanotrench ablation on carbon nanotubes. , 2017, , .		0

#	Article	lF	CITATIONS
91	Micrometer-Scale Magnetic-Resonance-Coupled Radio-Frequency Identification and Transceivers for Wireless Sensors in Cells. Physical Review Applied, 2017, 8, .	1.5	18
92	Transforming nanodevices to next generation nanosystems. , 2016, , .		0
93	32-bit Processor core at 5-nm technology: Analysis of transistor and interconnect impact on VLSI system performance. , 2016, , .		26
94	Hyperdimensional computing with 3D VRRAM in-memory kernels: Device-architecture co-design for energy-efficient, error-resilient language recognition. , 2016, , .		95
95	Microsecond transient thermal behavior of HfOx-based resistive random access memory using a micro thermal stage (MTS). , 2016, , .		10
96	High-Performance p-Type Black Phosphorus Transistor with Scandium Contact. ACS Nano, 2016, 10, 4672-4677.	7.3	119
97	A Compact Model for Metal–Oxide Resistive Random Access Memory With Experiment Verification. IEEE Transactions on Electron Devices, 2016, 63, 1884-1892.	1.6	163
98	Four-layer 3D vertical RRAM integrated with FinFET as a versatile computing unit for brain-inspired cognitive information processing. , 2016, , .		48
99	MoS ₂ transistors with 1-nanometer gate lengths. Science, 2016, 354, 99-102.	6.0	1,140
100	Picosecond Electric-Field-Induced Threshold Switching in Phase-Change Materials. Physical Review Letters, 2016, 117, 067601.	2.9	59
101	Distinctive in-Plane Cleavage Behaviors of Two-Dimensional Layered Materials. ACS Nano, 2016, 10, 8980-8988.	7.3	90
102	High Current Density and Low Thermal Conductivity of Atomically Thin Semimetallic WTe ₂ . ACS Nano, 2016, 10, 7507-7514.	7.3	100
103	Engineering a Large Scale Indium Nanodot Array for Refractive Index Sensing. ACS Applied Materials & Interfaces, 2016, 8, 31871-31877.	4.0	13
104	Memory — The N3XT frontier. , 2016, , .		0
105	Neuromorphic architectures with electronic synapses. , 2016, , .		26
106	Disturbance characteristics of half-selected cells in a cross-point resistive switching memory array. Nanotechnology, 2016, 27, 215204.	1.3	5
107	Hysteresis in Carbon Nanotube Transistors: Measurement and Analysis of Trap Density, Energy Level, and Spatial Distribution. ACS Nano, 2016, 10, 4599-4608.	7.3	62
108	Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 577-586.	3.5	20

#	Article	IF	CITATIONS
109	Removable and Recyclable Conjugated Polymers for Highly Selective and High-Yield Dispersion and Release of Low-Cost Carbon Nanotubes. Journal of the American Chemical Society, 2016, 138, 802-805.	6.6	152
110	Statistical Study on the Schottky Barrier Reduction of Tunneling Contacts to CVD Synthesized MoS ₂ . Nano Letters, 2016, 16, 276-281.	4.5	156
111	Efficient metallic carbon nanotube removal for highly-scaled technologies. , 2015, , .		25
112	Memory Devices: In Situ Tuning of Switching Window in a Gate-Controlled Bilayer Graphene-Electrode Resistive Memory Device (Adv. Mater. 47/2015). Advanced Materials, 2015, 27, 7766-7766.	11.1	1
113	In Situ Tuning of Switching Window in a Gateâ€Controlled Bilayer Grapheneâ€Electrode Resistive Memory Device. Advanced Materials, 2015, 27, 7767-7774.	11.1	54
114	Partitioning Electrostatic and Mechanical Domains in Nanoelectromechanical Relays. Journal of Microelectromechanical Systems, 2015, 24, 592-598.	1.7	8
115	Largeâ€Area Assembly of Densely Aligned Singleâ€Walled Carbon Nanotubes Using Solution Shearing and Their Application to Fieldâ€Effect Transistors. Advanced Materials, 2015, 27, 2656-2662.	11.1	123
116	Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1082-1095.	1.9	36
117	Cu diffusion barrier: Graphene benchmarked to TaN for ultimate interconnect scaling. , 2015, , .		16
118	Energy-Efficient Abundant-Data Computing: The N3XT 1,000x. Computer, 2015, 48, 24-33.	1.2	156
119	A General Design Strategy for Block Copolymer Directed Self-Assembly Patterning of Integrated Circuits Contact Holes using an Alphabet Approach. Nano Letters, 2015, 15, 805-812.	4.5	41
120	Memory leads the way to better computing. Nature Nanotechnology, 2015, 10, 191-194.	15.6	671
121	Physical Layout Design of Directed Self-Assembly Guiding Alphabet for IC Contact Hole/via Patterning. , 2015, , .		3
122	Vertical and Lateral Copper Transport through Graphene Layers. ACS Nano, 2015, 9, 8361-8367.	7.3	31
123	1D Selection Device Using Carbon Nanotube FETs for High-Density Cross-Point Memory Arrays. IEEE Transactions on Electron Devices, 2015, 62, 2197-2204.	1.6	34
124	Metal oxide-resistive memory using graphene-edge electrodes. Nature Communications, 2015, 6, 8407.	5.8	127
125	Compact modeling and design optimization of carbon nanotube field-effect transistors for the sub-10-nm technology nodes. , 2015, , .		4
126	Layout optimization and template pattern verification for directed self-assembly (DSA). , 2015, , .		2

#	Article	IF	CITATIONS
127	3-D Resistive Memory Arrays: From Intrinsic Switching Behaviors to Optimization Guidelines. IEEE Transactions on Electron Devices, 2015, 62, 3160-3167.	1.6	16
128	Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier. Nano Letters, 2015, 15, 6809-6814.	4.5	121
129	RRAM based synaptic devices for neuromorphic visual systems. , 2015, , .		5
130	3D RRAM: Design and optimization. , 2014, , .		3
131	Statistical assessment methodology for the design and optimization of cross-point RRAM arrays. , 2014, , .		10
132	Ultrathin (∼2nm) HfO <inf>x</inf> as the fundamental resistive switching element: Thickness scaling limit, stack engineering and 3D integration. , 2014, , .		12
133	Capacity optimization of emerging memory systems: A shannon-inspired approach to device characterization. , 2014, , .		4
134	Robust design and experimental demonstrations of carbon nanotube digital circuits. , 2014, , .		3
135	System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-19.	1.8	8
136	DSA-aware detailed routing for via layer optimization. , 2014, , .		13
137	DSA template optimization for contact layer in 1D standard cell design. , 2014, , .		11
138	GaAs buffer layer technique for vertical nanowire growth on Si substrate. Applied Physics Letters, 2014, 104, 083113.	1.5	1
139	Ultrafast terahertz-induced response of GeSbTe phase-change materials. Applied Physics Letters, 2014, 104, .	1.5	38
140	Improved multi-level control of RRAM using pulse-train programming. , 2014, , .		6
141	Characterization and Modeling of the Conduction and Switching Mechanisms of HfO _x Based RRAM. Materials Research Society Symposia Proceedings, 2014, 1631, 1.	0.1	6
142	Atomically thin graphene plane electrode for 3D RRAM. , 2014, , .		12
143	Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs. , 2014, , .		105

144 High-performance carbon nanotube field-effect transistors. , 2014, , .

#	Article	IF	CITATIONS
145	3-D Cross-Point Array Operation on <inline-formula> <tex-math notation="TeX">\${m AlO}_{y}/{m HfO}_{x}\$ </tex-math></inline-formula> -Based Vertical Resistive Switching Memory. IEEE Transactions on Electron Devices, 2014, 61, 1377-1381.	1.6	22
146	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	3.5	101
147	Impact of pulse rise time on programming of cross-point RRAM arrays. , 2014, , .		0
148	Cross plane thermal conductance of graphene-metal interfaces. , 2014, , .		7
149	Carbon nanotubes for high-performance logic. MRS Bulletin, 2014, 39, 719-726.	1.7	11
150	Design guidelines for 3D RRAM cross-point architecture. , 2014, , .		17
151	Multi-level control of conductive nano-filament evolution in HfO ₂ ReRAM by pulse-train operations. Nanoscale, 2014, 6, 5698-5702.	2.8	137
152	The Role of Ti Capping Layer in HfO _{<italic>x</italic>} -Based RRAM Devices. IEEE Electron Device Letters, 2014, 35, 912-914.	2.2	55
153	Ultrafast Characterization of Phase-Change Material Crystallization Properties in the Melt-Quenched Amorphous Phase. Nano Letters, 2014, 14, 3419-3426.	4.5	102
154	Continuous wireless pressure monitoring and mapping with ultra-small passive sensors for health monitoring and critical care. Nature Communications, 2014, 5, 5028.	5.8	418
155	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	7.3	70
156	Ultra-Low-Energy Three-Dimensional Oxide-Based Electronic Synapses for Implementation of Robust High-Accuracy Neuromorphic Computation Systems. ACS Nano, 2014, 8, 6998-7004.	7.3	172
157	Cost-Effective, Transfer-Free, Flexible Resistive Random Access Memory Using Laser-Scribed Reduced Graphene Oxide Patterning Technology. Nano Letters, 2014, 14, 3214-3219.	4.5	114
158	Monolithic three-dimensional integration of carbon nanotube FETs with silicon CMOS. , 2014, , .		21
159	VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-Function Metal Oxides. Nano Letters, 2014, 14, 1884-1890.	4.5	63
160	Brain-like associative learning using a nanoscale non-volatile phase change synaptic device array. Frontiers in Neuroscience, 2014, 8, 205.	1.4	176
161	Atomic layer deposition of high- <i>k</i> dielectrics on single-walled carbon nanotubes: a Raman study. Nanotechnology, 2013, 24, 245703.	1.3	19
162	Combinational Logic Design Using Six-Terminal NEM Relays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 653-666.	1.9	32

#	Article	IF	CITATIONS
163	Carbon nanotube computer. Nature, 2013, 501, 526-530.	13.7	903
164	Synaptic electronics: materials, devices and applications. Nanotechnology, 2013, 24, 382001.	1.3	1,012
165	Carbon Nanotube Circuits: Opportunities and Challenges. , 2013, , .		3
166	Compact models of emerging devices. , 2013, , .		0
167	Phonon and electron transport through Ge2Sb2Te5 films and interfaces bounded by metals. Applied Physics Letters, 2013, 102, .	1.5	68
168	Block copolymer directed self-assembly (DSA) aware contact layer optimization for 10 nm 1D standard cell library. , 2013, , .		31
169	Synergetic carbon nanotube growth. Carbon, 2013, 62, 61-68.	5.4	5
170	Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length. IEEE Transactions on Electron Devices, 2013, 60, 1834-1843.	1.6	64
171	HfO _x -Based Vertical Resistive Switching Random Access Memory Suitable for Bit-Cost-Effective Three-Dimensional Cross-Point Architecture. ACS Nano, 2013, 7, 2320-2325.	7.3	309
172	Monitoring Oxygen Movement by Raman Spectroscopy of Resistive Random Access Memory with a Graphene-Inserted Electrode. Nano Letters, 2013, 13, 651-657.	4.5	121
173	Experimental study of plane electrode thickness scaling for 3D vertical resistive random access memory. Nanotechnology, 2013, 24, 465201.	1.3	24
174	First demonstration of RRAM patterned by block copolymer self-assembly. , 2013, , .		6
175	Impact of Ill–V and Ge Devices on Circuit Performance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1189-1200.	2.1	Ο
176	Nanometer-Scale \${m HfO}_{x}\$ RRAM. IEEE Electron Device Letters, 2013, 34, 1005-1007.	2.2	51
177	Design and optimization methodology for 3D RRAM arrays. , 2013, , .		36
178	Monolithic three-dimensional integration of carbon nanotube FET complementary logic circuits. , 2013, , .		19
179	Experimental demonstration of array-level learning with phase change synaptic devices. , 2013, , .		35
180	A Low Energy Oxideâ€Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation. Advanced Materials, 2013, 25, 1774-1779.	11.1	445

#	Article	IF	CITATIONS
181	Single-Tube Characterization Methodology for Experimental and Analytical Evaluation of Carbon Nanotube Synthesis. Japanese Journal of Applied Physics, 2012, 51, 04DB02.	0.8	0
182	Electrothermal Modeling and Design Strategies for Multibit Phase-Change Memory. IEEE Transactions on Electron Devices, 2012, 59, 3561-3567.	1.6	28
183	Electrode/oxide interface engineering by inserting single-layer graphene: Application for HfO <inf>x</inf> -based resistive random access memory. , 2012, , .		12
184	Optical Absorption Enhancement: Optical Absorption Enhancement in Freestanding GaAs Thin Film Nanopyramid Arrays (Adv. Energy Mater. 10/2012). Advanced Energy Materials, 2012, 2, 1150-1150.	10.2	7
185	Low-Energy Robust Neuromorphic Computation Using Synaptic Devices. IEEE Transactions on Electron Devices, 2012, 59, 3489-3494.	1.6	76
186	Scaling behavior of PCM cells in off-state conduction. , 2012, , .		3
187	Electrical properties of CuPc-based OTFTs with atomic layer deposited HfAlO gate dielectric. , 2012, , .		0
188	Recent progress of resistive switching random access memory (RRAM). , 2012, , .		10
189	HfOx based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector. , 2012, , .		106
190	A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations. IEEE Electron Device Letters, 2012, 33, 1405-1407.	2.2	212
191	Metal–Oxide RRAM. Proceedings of the IEEE, 2012, 100, 1951-1970.	16.4	2,225
192	Selective Synthesis and Device Applications of Semiconducting Single-Walled Carbon Nanotubes Using Isopropyl Alcohol as Feedstock. ACS Nano, 2012, 6, 7454-7462.	7.3	107
193	Metal Oxide Resistive Switching Memory. Springer Series in Materials Science, 2012, , 303-335.	0.4	17
194	Resistive switching random access memory — Materials, device, interconnects, and scaling considerations. , 2012, , .		0
195	Nano-Electro-Mechanical relays for FPGA routing: Experimental demonstration and a design technique. , 2012, , .		28
196	Graphene Interconnect Lifetime: A Reliability Analysis. IEEE Electron Device Letters, 2012, 33, 1604-1606.	2.2	30
197	Graphene interconnect lifetime under high current stress. , 2012, , .		3
198	Nanoscale phase change memory materials. Nanoscale, 2012, 4, 4382.	2.8	61

#	Article	IF	CITATIONS
199	Variability in Carbon Nanotube Transistors: Improving Device-to-Device Consistency. ACS Nano, 2012, 6, 1109-1115.	7.3	115
200	Phase Change Memory: Scaling and applications. , 2012, , .		11
201	Increasing the semiconducting fraction in ensembles of single-walled carbon nanotubes. Carbon, 2012, 50, 5093-5098.	5.4	10
202	A Monte Carlo study of the low resistance state retention of HfOx based resistive switching memory. Applied Physics Letters, 2012, 100, .	1.5	60
203	Effect of annealing ambient and temperature on the electrical characteristics of atomic layer deposition Al2O3/In0.53Ga0.47As metal-oxide-semiconductor capacitors and MOSFETs. Journal of Applied Physics, 2012, 111, .	1.1	40
204	A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling. , 2012, , .		148
205	On the Switching Parameter Variation of Metal-Oxide RRAM—Part I: Physical Modeling and Simulation Methodology. IEEE Transactions on Electron Devices, 2012, 59, 1172-1182.	1.6	300
206	Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing. Nano Letters, 2012, 12, 2179-2186.	4.5	1,036
207	Flexible Control of Block Copolymer Directed Selfâ€Assembly using Small, Topographical Templates: Potential Lithography Solution for Integrated Circuit Contact Hole Patterning. Advanced Materials, 2012, 24, 3107-3114.	11.1	112
208	Template Patterning: Flexible Control of Block Copolymer Directed Self-Assembly using Small, Topographical Templates: Potential Lithography Solution for Integrated Circuit Contact Hole Patterning (Adv. Mater. 23/2012). Advanced Materials, 2012, 24, 3082-3082.	11.1	2
209	Optical Absorption Enhancement in Freestanding GaAs Thin Film Nanopyramid Arrays. Advanced Energy Materials, 2012, 2, 1254-1260.	10.2	52
210	Carbon Nanotube Robust Digital VLSI. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 453-471.	1.9	104
211	An Ultra-Low Reset Current Cross-Point Phase Change Memory With Carbon Nanotube Electrodes. IEEE Transactions on Electron Devices, 2012, 59, 1155-1163.	1.6	79
212	On the Switching Parameter Variation of Metal Oxide RRAM—Part II: Model Corroboration and Device Design Strategy. IEEE Transactions on Electron Devices, 2012, 59, 1183-1188.	1.6	196
213	Single-Tube Characterization Methodology for Experimental and Analytical Evaluation of Carbon Nanotube Synthesis. Japanese Journal of Applied Physics, 2012, 51, 04DB02.	0.8	0
214	SRAM, NAND, DRAM contact hole patterning using block copolymer directed self-assembly guided by small topographical templates. , 2011, , .		28
215	First demonstration of phase change memory device using solution processed GeTe nanoparticles. , 2011, , .		9

#	Article	IF	CITATIONS
217	Grain Boundaries, Phase Impurities, and Anisotropic Thermal Conduction in Phase-Change Memory. IEEE Electron Device Letters, 2011, 32, 961-963.	2.2	16
218	2D analytical model for the study of NEM relay device scaling. , 2011, , .		3
219	Complex Band Structures: From Parabolic to Elliptic Approximation. IEEE Electron Device Letters, 2011, 32, 1296-1298.	2.2	24
220	<i>In Situ</i> Transmission Electron Microscopy Observation of Nanostructural Changes in Phase-Change Memory. ACS Nano, 2011, 5, 2742-2748.	7.3	48
221	Impact of fixed charge on metal-insulator-semiconductor barrier height reduction. Applied Physics Letters, 2011, 99, .	1.5	54
222	Viability Study of All-III–V SRAM for Beyond-22-nm Logic Circuits. IEEE Electron Device Letters, 2011, 32, 877-879.	2.2	3
223	Experimental demonstration of In0.53Ga0.47As field effect transistors with scalable nonalloyed source/drain contacts. Applied Physics Letters, 2011, 98, .	1.5	13
224	Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. , 2011, , .		49
225	Overcoming carbon nanotube variations through co-optimized technology and circuit design. , 2011, , .		27
226	Carbon nanotube electronics - Materials, devices, circuits, design, modeling, and performance projection. , 2011, , .		22
227	AC conductance measurement and analysis of the conduction processes in HfOx based resistive switching memory. Applied Physics Letters, 2011, 99, .	1.5	31
228	On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, monte carlo simulation, and experimental characterization. , 2011, , .		138
229	Conduction mechanism of TiN/HfOx/Pt resistive switching memory: A trap-assisted-tunneling model. Applied Physics Letters, 2011, 99, .	1.5	327
230	Novel contact structures for high mobility channel materials. MRS Bulletin, 2011, 36, 112-120.	1.7	8
231	Recent Progress of Phase Change Memory (PCM) and Resistive Switching Random Access Memory (RRAM). , 2011, , .		6
232	Electronic and optical switching of solution-phase deposited SnSe2 phase change memory material. Journal of Applied Physics, 2011, 109, .	1.1	51
233	Characterization and Design of Logic Circuits in the Presence of Carbon Nanotube Density Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1103-1113.	1.9	41
234	Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage. IEEE Transactions on Electron Devices, 2011, 58, 584-592.	1.6	58

#	Article	IF	CITATIONS
235	Physics-Based Compact Model for III–V Digital Logic FETs Including Gate Tunneling Leakage and Parasitic Capacitance. IEEE Transactions on Electron Devices, 2011, 58, 1068-1075.	1.6	10
236	Compact Modeling of Conducting-Bridge Random-Access Memory (CBRAM). IEEE Transactions on Electron Devices, 2011, 58, 1352-1360.	1.6	207
237	The Effect of Donor/Acceptor Nature of Interface Traps on Ge MOSFET Characteristics. IEEE Transactions on Electron Devices, 2011, 58, 1015-1022.	1.6	57
238	One-Dimensional Thickness Scaling Study of Phase Change Material \$(hbox{Ge}_{2}hbox{Sb}_{2}hbox{Te}_{5})\$ Using a Pseudo 3-Terminal Device. IEEE Transactions on Electron Devices, 2011, 58, 1483-1489.	1.6	24
239	Parasitic Capacitances: Analytical Models and Impact on Circuit-Level Performance. IEEE Transactions on Electron Devices, 2011, 58, 1361-1370.	1.6	42
240	An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation. IEEE Transactions on Electron Devices, 2011, 58, 2729-2737.	1.6	731
241	Noniterative Compact Modeling for Intrinsic Carbon-Nanotube FETs: Quantum Capacitance and Ballistic Transport. IEEE Transactions on Electron Devices, 2011, 58, 2456-2465.	1.6	20
242	Technology Assessment Methodology for Complementary Logic Applications Based on Energy–Delay Optimization. IEEE Transactions on Electron Devices, 2011, 58, 2430-2439.	1.6	11
243	Fabrication and Characterization of Nanoscale NiO Resistance Change Memory (RRAM) Cells With Confined Conduction Paths. IEEE Transactions on Electron Devices, 2011, 58, 3270-3275.	1.6	13
244	Nanoscale Bipolar and Complementary Resistive Switching Memory Based on Amorphous Carbon. IEEE Transactions on Electron Devices, 2011, 58, 3933-3939.	1.6	78
245	Investigation of Trap Spacing for the Amorphous State of Phase-Change Memory Devices. IEEE Transactions on Electron Devices, 2011, 58, 4370-4376.	1.6	12
246	Crystallization properties and their drift dependence in phase-change memory studied with a micro-thermal stage. Journal of Applied Physics, 2011, 110, .	1.1	15
247	Tight-binding study of Γ-L bandstructure engineering for ballistic III–V nMOSFETs. , 2011, ,		1
248	Microthermal Stage for Electrothermal Characterization of Phase-Change Memory. IEEE Electron Device Letters, 2011, 32, 952-954.	2.2	11
249	Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory. Applied Physics Letters, 2011, 98, .	1.5	245
250	Direct Measurement of Trap Spacing in Phase Change Memory Cells Using ATE Devices. , 2011, , .		1
251	Metal/III–V effective barrier height tuning using ALD high-κ dipoles. , 2011, , .		3
252	Carbon electronics — From material synthesis to circuit demonstration. , 2011, , .		1

#	Article	IF	CITATIONS
253	Air-stable technique for fabricating n-type carbon nanotube FETs. , 2011, , .		10
254	Metal/III-V effective barrier height tuning using atomic layer deposition of high-κ/high-κ bilayer interfaces. Applied Physics Letters, 2011, 99, 092107.	1.5	36
255	Carbon nanotube imperfection-immune digital VLSI: Frequently asked questions updated. , 2011, , .		4
256	Carbon-Based Nanomaterial for Nanoelectronics. ECS Transactions, 2011, 35, 259-269.	0.3	3
257	Imperfection-Immune Carbon Nanotube VLSI Circuits. , 2011, , 277-305.		2
258	SLICE image analysis for diblock copolymer characterization and process optimization. , 2010, , .		0
259	Carbon nanotube correlation. , 2010, , .		48
260	Uniaxial Stress Engineering for High-Performance Ge NMOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 1037-1046.	1.6	29
261	ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon Nanotube VLSI: Analyses and Design Guidelines. IEEE Transactions on Electron Devices, 2010, 57, 2284-2295.	1.6	22
262	Cross-Point Memory Array Without Cell Selectors—Device Characteristics and Data Storage Pattern Dependencies. IEEE Transactions on Electron Devices, 2010, 57, 2531-2538.	1.6	241
263	Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics. IEEE Transactions on Electron Devices, 2010, 57, 3137-3143.	1.6	127
264	Phase Change Memory. Proceedings of the IEEE, 2010, 98, 2201-2227.	16.4	1,420
265	Metal/III-V Schottky barrier height tuning for the design of nonalloyed III-V field-effect transistor source/drain contacts. Journal of Applied Physics, 2010, 107, .	1.1	75
266	Performance benchmarks for Si, III–V, TFET, and carbon nanotube FET - re-thinking the technology assessment methodology for complementary logic applications. , 2010, , .		18
267	Monolithic III–V nanowire PV for photoelectrochemical hydrogen generation. , 2010, , .		0
268	Size limitation of cross-point memory array and its dependence on data storage pattern and device parameters. , 2010, , .		12
269	Recent progress of phase change memory (PCM) and resistive switching random access memory (RRAM). , 2010, , .		10
270	Carbon nanotube circuits: Living with imperfections and variations. , 2010, , .		11

16

#	Article	IF	CITATIONS
271	A Phenomenological Model for the Reset Mechanism of Metal Oxide RRAM. IEEE Electron Device Letters, 2010, 31, 1455-1457.	2.2	183
272	Read/write schemes analysis for novel complementary resistive switches in passive crossbar memory arrays. Nanotechnology, 2010, 21, 465202.	1.3	57
273	Efficient FPGAs using nanoelectromechanical relays. , 2010, , .		62
274	Spectroscopic Evidence for Exceptional Thermal Contribution to Electron Beam-Induced Fragmentation. Journal of Physical Chemistry C, 2010, 114, 22064-22068.	1.5	7
275	<pre>\$hbox{Al}_{2}hbox{O}_{3}\$-Based RRAM Using Atomic Layer Deposition (ALD) With 1-\$muhbox{A}\$ RESET Current. IEEE Electron Device Letters, 2010, 31, 1449-1451.</pre>	2.2	142
276	Synthesis and size-dependent crystallization of colloidal germanium telluridenanoparticles. Journal of Materials Chemistry, 2010, 20, 1285-1291.	6.7	114
277	Titanium nitride sidewall stringer process for lateral nanoelectromechanical relays. , 2010, , .		8
278	Modeling the switching dynamics of programmable-metallization-cell (PMC) memory and its application as synapse device for a neuromorphic computation system. , 2010, , .		30
279	Device and circuit interactive design and optimization beyond the conventional scaling era. , 2010, , .		1
280	Ultra-low power Al <inf>2</inf> O <inf>3</inf> -based RRAM with 1μA reset current. , 2010, , .		16
281	Decoupled thermal resistances of phase change material and their impact on PCM devices. , 2010, , .		3
282	Modeling and analysis of III–V logic FETs for devices and circuits: Sub-22nm technology III–V SRAM cell design. , 2010, , .		0
283	A phenomenological model of oxygen ion transport for metal oxide resistive switching memory. , 2010, , .		10
284	Thermal Boundary Resistance Measurements for Phase-Change Memory Devices. IEEE Electron Device Letters, 2010, 31, 56-58.	2.2	105
285	Thermal disturbance and its impact on reliability of phase-change memory studied by the micro-thermal stage. , 2010, , .		26
286	Current Scaling in Aligned Carbon Nanotube Array Transistors With Local Bottom Gating. IEEE Electron Device Letters, 2010, 31, 644-646.	2.2	37
287	Metal-induced dopant (boron and phosphorus) activation process in amorphous germanium for monolithic three-dimensional integration. Journal of Applied Physics, 2009, 106, .	1.1	18
288	Analog Nanoelectromechanical Relay With Tunable Transconductance. IEEE Electron Device Letters, 2009, 30, 1143-1145.	2.2	10

#	Article	IF	CITATIONS
289	Crystallization times of Ge–Te phase change materials as a function of composition. Applied Physics Letters, 2009, 95, .	1.5	114
290	Measurement of Subnanosecond Delay Through Multiwall Carbon-Nanotube Local Interconnects in a CMOS Integrated Circuit. IEEE Transactions on Electron Devices, 2009, 56, 43-49.	1.6	16
291	Selective Device Structure Scaling and Parasitics Engineering: A Way to Extend the Technology Roadmap. IEEE Transactions on Electron Devices, 2009, 56, 312-320.	1.6	29
292	Effect of Parasitic Resistance and Capacitance on Performance of InGaAs HEMT Digital Logic Circuits. IEEE Transactions on Electron Devices, 2009, 56, 1161-1164.	1.6	9
293	ACCNT—A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration. IEEE Transactions on Electron Devices, 2009, 56, 2969-2978.	1.6	36
294	A Physics-Based Compact Model of III–V FETs for Digital Logic Applications: Current–Voltage and Capacitance–Voltage Characteristics. IEEE Transactions on Electron Devices, 2009, 56, 2917-2924.	1.6	20
295	Surface Science of Catalyst Dynamics for Aligned Carbon Nanotube Synthesis on a Full-Scale Quartz Wafer. Journal of Physical Chemistry C, 2009, 113, 8002-8008.	1.5	11
296	Measurement of anisotropy in the thermal conductivity of Ge <inf>2</inf> Sb <inf>2</inf> Te <inf>5</inf> films. , 2009, , .		1
297	Ultralow Voltage Crossbar Nonvolatile Memory Based on Energy-Reversible NEM Switches. IEEE Electron Device Letters, 2009, 30, 626-628.	2.2	38
298	A non-iterative compact model for carbon nanotube FETs incorporating source exhaustion effects. , 2009, , .		37
299	Fermi level depinning in metal/Ge Schottky junction for metal source/drain Ge metal-oxide-semiconductor field-effect-transistor application. Journal of Applied Physics, 2009, 105, .	1.1	165
300	Digital VLSI logic technology using Carbon Nanotube FETs. , 2009, , .		39
301	CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. Nano Letters, 2009, 9, 189-197.	4.5	161
302	Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits. IEEE Nanotechnology Magazine, 2009, 8, 37-45.	1.1	125
303	Threshold Voltage and On–Off Ratio Tuning for Multiple-Tube Carbon Nanotube FETs. IEEE Nanotechnology Magazine, 2009, 8, 4-9.	1.1	75
304	Carbon Nanotube Quantum Capacitance for Nonlinear Terahertz Circuits. IEEE Nanotechnology Magazine, 2009, 8, 31-36.	1.1	13
305	Carbon Nanotube Device Modeling and Circuit Simulation. Integrated Circuits and Systems, 2009, , 133-162.	0.2	7
306	Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes. IEEE Nanotechnology Magazine, 2009, 8, 498-504.	1.1	175

#	Article	IF	CITATIONS
307	Measuring Frequency Response of a Single-Walled Carbon Nanotube Common-Source Amplifier. IEEE Nanotechnology Magazine, 2009, 8, 226-233.	1.1	20
308	VMR: VLSI-compatible metallic carbon nanotube removal for imperfection-immune cascaded multi-stage digital logic circuits using Carbon Nanotube FETs. , 2009, , .		82
309	1D thickness scaling study of phase change material (Ge <inf>2</inf> Sb <inf>2</inf> Te <inf>5</inf>) using a pseudo 3-terminal device. , 2009, , .		12
310	Technology Projection Using Simple Compact Models. , 2009, , .		5
311	Top-gated FETs/inverters with diblock copolymer self-assembled 20 nm contact holes. , 2009, , .		2
312	Monolithic three-dimensional integrated circuits using carbon nanotube FETs and interconnects. , 2009, , .		9
313	Experimental demonstration of high mobility Ge NMOS. , 2009, , .		47
314	High-speed graphene interconnects monolithically integrated with CMOS ring oscillators operating at 1.3GHz. , 2009, , .		8
315	CMOS technology roadmap projection including parasitic effects. , 2009, , .		9
316	Fabrication and characterization of emerging nanoscale memory. , 2009, , .		4
317	Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage. , 2009, , .		58
318	Finite element analysis and analytical simulations of Suspended Gate-FET for ultra-low power inverters. Solid-State Electronics, 2008, 52, 1374-1381.	0.8	16
319	Analytical Modeling of the Suspended-Gate FET and Design Insights for Low-Power Logic. IEEE Transactions on Electron Devices, 2008, 55, 48-59.	1.6	71
320	An Analytical Derivation of the Density of States, Effective Mass, and Carrier Density for Achiral Carbon Nanotubes. IEEE Transactions on Electron Devices, 2008, 55, 289-297.	1.6	38
321	Integrating Phase-Change Memory Cell With Ge Nanowire Diode for Crosspoint Memory—Experimental Demonstration and Analysis. IEEE Transactions on Electron Devices, 2008, 55, 2307-2313.	1.6	20
322	Physics-based compact model of III-V heterostructure FETs for digital logic applications. , 2008, , .		10
323	Monolithic Integration of CMOS VLSI and Carbon Nanotubes for Hybrid Nanotechnology Applications. IEEE Nanotechnology Magazine, 2008, 7, 636-639.	1.1	40
324	A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors. Nano Letters, 2008, 8, 706-709.	4.5	185

#	Article	IF	CITATIONS
325	Assembly and Electrical Characterization of Multiwall Carbon Nanotube Interconnects. IEEE Nanotechnology Magazine, 2008, 7, 596-600.	1.1	28
326	The future of CMOS scaling - parasitics engineering and device footprint scaling. , 2008, , .		3
327	Carbon nanotube transistor compact model for circuit design and performance optimization. ACM Journal on Emerging Technologies in Computing Systems, 2008, 4, 1-20.	1.8	14
328	Integrated wafer-scale growth and transfer of directional Carbon Nanotubes and misaligned-Carbon-Nanotube-immune logic structures. , 2008, , .		45
329	Analytical ballistic theory of carbon nanotube transistors: Experimental validation, device physics, parameter extraction, and performance projection. Journal of Applied Physics, 2008, 104, 124514.	1.1	54
330	Sub-ns Delay Through Multi-Wall Carbon Nanotube Local Interconnects in a CMOS Integrated Circuit. , 2008, , .		0
331	Carrier density and quantum capacitance for semiconducting carbon nanotubes. Journal of Applied Physics, 2008, 104, .	1.1	27
332	Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1725-1736.	1.9	93
333	A Multi-Aperture Image Sensor With 0.7 \$mu{hbox{m}}\$ Pixels in 0.11 \$mu{hbox{m}}\$ CMOS Technology. IEEE Journal of Solid-State Circuits, 2008, 43, 2990-3005.	3.5	25
334	Energy-Reversible Complementary NEM Logic Gates. , 2008, , .		6
335	Analytical Degenerate Carrier Density and Quantum Capacitance for Semiconducting Carbon Nanotubes. , 2008, , .		Ο
336	Fermi-Level Depinning of GaAs for Ohmic Contacts. , 2008, , .		3
337	Monolithic integration of CMOS VLSI and CNT for hybrid nanotechnology applications. , 2008, , .		16
338	Low temperature (≤ 380°C) and high performance Ge CMOS technology with novel source/drain by metal-induced dopants activation and high-k/metal gate stack for monolithic 3D integration. , 2008, , .		36
339	Modeling of schottky and ohmic contacts between metal and graphene nanoribbons using extended hückel theory (EHT)-based NEGF method. , 2008, , .		6
340	Modeling and Performance Comparison of 1-D and 2-D Devices Including Parasitic Gate Capacitance and Screening Effect. IEEE Nanotechnology Magazine, 2008, 7, 720-727.	1.1	14
341	An analytical model for intrinsic carbon nanotube FETs. , 2008, , .		1
342	Extending Technology Roadmap by Selective Device Footprint Scaling and Parasitics Engineering. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	6

#	Article	IF	CITATIONS
343	Phase change nanodots patterning using a self-assembled polymer lithography and crystallization analysis. Journal of Applied Physics, 2008, 104, .	1.1	28
344	Crystallization Characteristics Of Phase Change Nanoparticle Arrays Fabricated By Self-Assembly Based Lithography. Materials Research Society Symposia Proceedings, 2008, 1072, 1.	0.1	0
345	Hole Mobility Characteristics under Electrical Stress for Surface-Channel Germanium Transistors with High-Î [®] Gate Stack. Japanese Journal of Applied Physics, 2008, 47, 2544-2547.	0.8	0
346	Device study, chemical doping, and logic circuits based on transferred aligned single-walled carbon nanotubes. Applied Physics Letters, 2008, 93, .	1.5	54
347	A 3MPixel Multi-Aperture Image Sensor with 0.7μm Pixels in 0.11μm CMOS. , 2008, , .		10
348	Diblock copolymer directed self-assembly for CMOS device fabrication. Proceedings of SPIE, 2008, , .	0.8	1
349	Scaling properties of phase change materials. , 2007, , .		12
350	1-D and 2-D Devices Performance Comparison Including Parasitic Gate Capacitance and Screening Effect. , 2007, , .		4
351	A 0.5 μm pixel frame-transfer CCD image sensor in 110 nm CMOS. , 2007, , .		6
352	Device Footprint Scaling for Ultra Thin Body Fully Depleted SOI. , 2007, , .		0
353	Analysis of Temperature in Phase Change Memory Scaling. IEEE Electron Device Letters, 2007, 28, 697-699.	2.2	46
354	Band to Band Tunneling Study in High Mobility Materials : III-V, Si, Ge and strained SiGe. , 2007, , .		18
355	Synthesis of Metal Chalcogenide Nanodot Arrays Using Block Copolymer-Derived Nanoreactors. Nano Letters, 2007, 7, 3504-3507.	4.5	17
356	An Integrated Phase Change Memory Cell With Ge Nanowire Diode For Cross-Point Memory. , 2007, , .		33
357	Modeling Carbon Nanotube Sensors. IEEE Sensors Journal, 2007, 7, 1356-1357.	2.4	9
358	Fabrication and Characterization of Carbon Nanotube Interconnects. , 2007, , .		27
359	Biomimetic Approaches for Fabricating High-Density Nanopatterned Arrays. Chemistry of Materials, 2007, 19, 839-843.	3.2	33
360	Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	91

#	Article	IF	CITATIONS
361	Analytical Model of Carbon Nanotube Electrostatics: Density of States, Effective Mass, Carrier Density, and Quantum Capacitance. , 2007, , .		3
362	Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films. Applied Physics Letters, 2007, 91, .	1.5	112
363	Phase change nanodot arrays fabricated using a self-assembly diblock copolymer approach. Applied Physics Letters, 2007, 91, 013104.	1.5	35
364	Schottky-Barrier Carbon Nanotube Field-Effect Transistor Modeling. IEEE Transactions on Electron Devices, 2007, 54, 439-445.	1.6	59
365	A Composite Circuit Model for NDR Devices in Random Access Memory Cells. IEEE Transactions on Electron Devices, 2007, 54, 776-783.	1.6	4
366	The Impact of Device Footprint Scaling on High-Performance CMOS Logic Technology. IEEE Transactions on Electron Devices, 2007, 54, 1148-1155.	1.6	13
367	Impact of a Process Variation on Nanowire and Nanotube Device Performance. IEEE Transactions on Electron Devices, 2007, 54, 2369-2376.	1.6	98
368	Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET With Multiple Cylindrical Conducting Channels. IEEE Transactions on Electron Devices, 2007, 54, 2377-2385.	1.6	106
369	A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region. IEEE Transactions on Electron Devices, 2007, 54, 3186-3194.	1.6	715
370	A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking. IEEE Transactions on Electron Devices, 2007, 54, 3195-3205.	1.6	587
371	A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors. , 2006, , .		74
372	First Demonstration of AC Gain From a Single-walled Carbon Nanotube Common-Source Amplifier. , 2006, , .		25
373	Analysis of the Frequency Response of Carbon Nanotube Transistors. IEEE Nanotechnology Magazine, 2006, 5, 599-605.	1.1	34
374	Research opportunities for nanoscale CMOS. , 2006, , .		0
375	A 3D Multi-Aperture Image Sensor Architecture. , 2006, , .		33
376	Carbon Nanotube Transistor Circuits - Models and Tools for Design and Performance Optimization. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
377	Diblock copolymer directed self-assembly for CMOS device fabrication. , 2006, 6156, 329.		12
378	Metrics for performance benchmarking of nanoscale Si and carbon nanotube FETs including device nonidealities. IEEE Transactions on Electron Devices, 2006, 53, 1317-1322.	1.6	23

#	Article	IF	CITATIONS
379	Carbon nanotube transistor circuits. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	15
380	Beyond the conventional transistor. Solid-State Electronics, 2005, 49, 755-762.	0.8	81
381	The end of CMOS scaling. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2005, 21, 16-26.	0.8	361
382	Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation With Ni. IEEE Transactions on Electron Devices, 2004, 51, 2115-2120.	1.6	53
383	Frequency Response of Top-Gated Carbon Nanotube Field-Effect Transistors. IEEE Nanotechnology Magazine, 2004, 3, 383-387.	1.1	46
384	Self-Aligned n-Channel Germanium MOSFETs With a Thin Ge Oxynitride Gate Dielectric and Tungsten Gate. IEEE Electron Device Letters, 2004, 25, 135-137.	2.2	161
385	Two gates are better than one [double-gate MOSFET process]. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2003, 19, 48-62.	0.8	63
386	Strained Si CMOS (SS CMOS) technology: opportunities and challenges. Solid-State Electronics, 2003, 47, 1133-1139.	0.8	82
387	Extension and source/drain design for high-performance finFET devices. IEEE Transactions on Electron Devices, 2003, 50, 952-958.	1.6	266
388	Electrical characterization of germanium p-channel MOSFETs. IEEE Electron Device Letters, 2003, 24, 242-244.	2.2	160
389	An experimental study on transport issues and electrostatics of ultrathin body SOI pMOSFETs. IEEE Electron Device Letters, 2002, 23, 609-611.	2.2	22
390	Electron and hole mobility enhancement in strained SOI by wafer bonding. IEEE Transactions on Electron Devices, 2002, 49, 1566-1571.	1.6	51
391	SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors. Applied Physics Letters, 2001, 78, 1267-1269.	1.5	112
392	Modeling the Impact of Body-to-body Leakage in Partially-Depleted SOI CMOS Technology. , 2001, , 230-233.		2
393	Analysis of the design space available for high-kgate dielectrics in nanoscale MOSFETs. Superlattices and Microstructures, 2000, 28, 485-491.	1.4	12
394	Characterization of the silicon on insulator film in bonded wafers by high resolution x-ray diffraction. Applied Physics Letters, 1999, 75, 787-789.	1.5	35
395	Transient Enhanced Diffusion and Dose Loss of Indium in Silicon. Materials Research Society Symposia Proceedings, 1999, 568, 205.	0.1	18
396	Discrete random dopant distribution effects in nanometer-scale MOSFETs. Microelectronics Reliability, 1998, 38, 1447-1456.	0.9	70

#	Article	IF	CITATIONS
397	CMOS active pixel image sensors fabricated using a 1.8-V, 0.25-μm CMOS technology. IEEE Transactions on Electron Devices, 1998, 45, 889-894.	1.6	60
398	Monitoring hot-carrier degradation in SOI MOSFETs by hot-carrier luminescence techniques. IEEE Transactions on Electron Devices, 1998, 45, 1135-1139.	1.6	8
399	Digital Imaging. IEEE Micro, 1998, 18, 12-13.	1.8	3
400	Generalized scale length for two-dimensional effects in MOSFETs. IEEE Electron Device Letters, 1998, 19, 385-387.	2.2	278
401	Fabrication of ultrathin, highly uniform thin-film SOI MOSFETs with low series resistance using pattern-constrained epitaxy. IEEE Transactions on Electron Devices, 1997, 44, 1131-1135.	1.6	8
402	Technology and device scaling considerations for CMOS imagers. IEEE Transactions on Electron Devices, 1996, 43, 2131-2142.	1.6	211
403	Scaling silicon MOS devices to their limits. Microelectronic Engineering, 1996, 32, 271-282.	1.1	13
404	Gate current injection in MOSFET's with a split-gate (virtual drain) structure. IEEE Electron Device Letters, 1993, 14, 262-264.	2.2	3
405	TDI charge-coupled devices: Design and applications. IBM Journal of Research and Development, 1992, 36, 83-106.	3.2	81
406	Experimental verification of the mechanism of hot-carrier-induced photon emission in n-MOSFETs using an overlapping CCD gate structure. IEEE Electron Device Letters, 1992, 13, 389-391.	2.2	8
407	Effect of knife-edge skew on modulation transfer function measurement of charge-coupled device imagers employing a scanning knife edge. Optical Engineering, 1991, 30, 1394.	0.5	30
408	A CMOS-integrated 'ISFET-operational amplifier' chemical sensor employing differential sensing. IEEE Transactions on Electron Devices, 1989, 36, 479-487.	1.6	83
409	Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel. , 0, , .		166
410	Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. , 0, , .		165
411	Investigation of the performance limits of III-V double-gate n-MOSFETs. , 0, , .		28
412	Carbon nanotube field-effect transistors. , 0, , 191-232.		0