Ulya R Karpuzcu

List of Publications by Year
in descending order

14 papers	236 citations	1478505 6 h-index	1372567 10 g-index
14 all docs	14 docs citations	14 times ranked	228 citing authors

#	Article	IF	Citations
1	CRAM-Seq: Accelerating RNA-Seq Abundance Quantification Using Computational RAM. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 2055-2071.	4.6	2
2	Trading Computation for Communication: A Taxonomy of Data Recomputation Techniques. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 496-506.	4.6	6
3	A Day In the Life of a Quantum Error. IEEE Computer Architecture Letters, 2021, 20, 13-16.	1.5	7
4	Exploring the Feasibility of Using 3-D XPoint as an In-Memory Computing Accelerator. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 88-96.	1.5	1
5	Special Issue on Quantum Computing. IEEE Micro, 2021, 41, 6-7.	1.8	0
6	Analyzing the Effects of Interconnect Parasitics in the STT CRAM In-Memory Computational Platform. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 71-79.	1.5	8
7	In-Memory Processing on the Spintronic CRAM: From Hardware Design to Application Mapping. IEEE Transactions on Computers, 2019, 68, 1159-1173.	3.4	69
8	POWERT Channels: A Novel Class of Covert CommunicationExploiting Power Management Vulnerabilities. , 2019, , .		17
9	Using Spin-Hall MTJs to Build an Energy-Efficient In-memory Computation Platform. , 2019, , .		26
10	Exploiting Algorithmic Noise Tolerance for Scalable On-Chip Voltage Regulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 229-242.	3.1	6
11	Mitigation of NBTI induced performance degradation in on-chip digital LDOs. , 2018, , .		9
12	Efficient In-Memory Processing Using Spintronics. IEEE Computer Architecture Letters, 2018, 17, 42-46.	1.5	49
13	Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing Among Distributed On-Chip Voltage Regulators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3019-3032.	3.1	12
14	Low-Cost Per-Core Voltage Domain Support for Power-Constrained High-Performance Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 747-758.	3.1	24