Sriseshan Srikanth

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/2014009/publications.pdf

Version: 2024-02-01

8 papers	39 citations	2682572 2 h-index	2550090 3 g-index
8 all docs	8 docs citations	8 times ranked	21 citing authors

#	Article	IF	Citations
1	The Superstrider Architecture: Integrating Logic and Memory Towards Non-Von Neumann Computing. , 2017, , .		10
2	Experimental Insights from the Rogues Gallery. , 2019, , .		8
3	Extending Mooreâ€™s Law via Computationally Error-Tolerant Computing. Transactions on Architecture and Code Optimization, 2018, 15, 1-27.	2.0	6
4	Scalable Energy-Efficient Microarchitectures With Computational Error Tolerance Via Redundant Residue Number Systems. IEEE Transactions on Computers, 2022, 71, 613-627.	3.4	4
5	Energy efficiency limits of logic and memory. , 2016, , .		3
6	Memory System Design for Ultra Low Power, Computationally Error Resilient Processor Microarchitectures. , 2018, , .		3
7	Merge Network for a Non-Von Neumann Accumulate Accelerator in a 3D Chip. , 2018, , .		3
8	SortCache. Transactions on Architecture and Code Optimization, 2021, 18, 1-24.	2.0	2