Ryan Kastner

List of Publications by Year
in descending order

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187	3,103	304743	330143
papers	citations	22 h-index	37 g-index

189	189	189	2025
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Remote Control System for Emergency Ventilators During SARS-CoV-2. IEEE Embedded Systems Letters, 2022, 14, 43-46.	1.9	9
2	Hardware Information Flow Tracking. ACM Computing Surveys, 2022, 54, 1-39.	23.0	25
3	ARTe: Providing real-time multitasking to Arduino. Journal of Systems and Software, 2022, 186, 111185.	4.5	1
4	Sherlock: A Multi-Objective Design Space Exploration Framework. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-20.	2.6	3
5	Integrating Information Flow Tracking into High-Level Synthesis Design Flow. , 2022, , 365-387.		1
6	Toward Hardware Security Property Generation at Scale. IEEE Security and Privacy, 2022, 20, 43-51.	1.2	3
7	A high-tech, low-cost, Internet of Things surfboard fin for coastal citizen science, outreach, and education. Continental Shelf Research, 2022, 242, 104748.	1.8	6
8	A multi-flow information flow tracking approach for proving quantitative hardware security properties. Tsinghua Science and Technology, 2021, 26, 62-71.	6.1	5
9	S2N2: A FPGA Accelerator for Streaming Spiking Neural Networks. , 2021, , .		28
10	A more precise way to localize animals using drones. Journal of Field Robotics, 2021, 38, 917-928.	6.0	10
11	Special Session: CAD for Hardware Security - Automation is Key to Adoption of Solutions. , 2021, , .		7
12	A UCSD view on replication and reproducibility for CPS & IoT. , 2021, , .		3
13	A Tunable Dual-Edge Time-to-Digital Converter. , 2021, , .		0
14	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	2.7	56
15	Classifying Computations on Multi-Tenant FPGAs. , 2021, , .		2
16	Isadora. , 2021, , .		4
17	iSTELLAR: intermittent Signature aTtenuation Embedded CRYPTO with Low-Level metAl Routing. , 2021, , .		0
18	Aker: A Design and Verification Framework for Safe and Secure SoC Access Control. , 2021, , .		18

#	Article	IF	Citations
19	Memory-Based High-Level Synthesis Optimizations Security Exploration on the Power Side-Channel. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2124-2137.	2.7	10
20	Real-time Automatic Modulation Classification using RFSoC. , 2020, , .		16
21	Low-cost 3D scanning systems for cultural heritage documentation. Journal of Cultural Heritage Management and Sustainable Development, 2020, 10, 437-455.	0.9	9
22	Target detection using features for sonar images. IET Radar, Sonar and Navigation, 2020, 14, 1940-1949.	1.8	14
23	FPGA Architectures for Real-time Dense SLAM. , 2019, , .		21
24	Holistic Power Side-Channel Leakage Assessment: Towards a Robust Multidimensional Metric. , 2019, , .		2
25	FastWave: Accelerating Autoregressive Convolutional Neural Networks on FPGA. , 2019, , .		13
26	D-SEA: The Underwater Depth Sensing Device for Standalone Time-Averaged Measurements. , 2019, , .		2
27	VeriSketch. , 2019, , .		8
28	Benchmarking Video with the Surgical Image Registration Generator (SIRGn) Baseline. Lecture Notes in Computer Science, 2019, , 320-331.	1.3	0
29	Self-Localization of a Deforming Swarm of Underwater Vehicles Using Impulsive Sound Sources of Opportunity. IEEE Access, 2018, 6, 1635-1646.	4.2	4
30	O(N)-Space Spatiotemporal Filter for Reducing Noise in Neuromorphic Vision Sensors. IEEE Transactions on Emerging Topics in Computing, 2018, , 1-1.	4.6	36
31	A hardware accelerated system for high throughput cellular image analysis. Journal of Parallel and Distributed Computing, 2018, 113, 167-178.	4.1	7
32	Examining the consequences of high-level synthesis optimizations on power side-channel. , 2018, , .		12
33	Quantitative Analysis of Timing Channel Security in Cryptographic Hardware Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1719-1732.	2.7	11
34	Property specific information flow analysis for hardware security verification. , 2018, , .		20
35	PynqCopter - An Open-source FPGA Overlay for UAVs. , 2018, , .		2
36	A Comparison of Feature Detectors for Underwater Sonar Imagery. , 2018, , .		7

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37	A FPGA Accelerator for Real-Time 3D Non-rigid Registration Using Tree Reweighted Message Passing and Dynamic Markov Random Field Generation. , 2018, , .		2
38	Everyone's a Critic: A Tool for Exploring RISC-V Projects. , 2018, , .		6
39	Self-localization of a mobile swarm using noise correlations with local sources of opportunity. Journal of the Acoustical Society of America, 2018, 144, 2811-2823.	1.1	3
40	Self-synchronization of multiple vehicles using ambient impulsive noise. , 2018, , .		0
41	Distributed compressed sensing based channel estimation for underwater acoustic multiband transmissions. Journal of the Acoustical Society of America, 2018, 143, 3985-3996.	1.1	23
42	Exploiting time varying sparsity for underwater acoustic communication via dynamic compressed sensing. Journal of the Acoustical Society of America, 2018, 143, 3997-4007.	1.1	20
43	Synthesizable Higher-Order Functions for C++. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2835-2844.	2.7	8
44	Symbolic execution based test-patterns generation algorithm for hardware Trojan detection. Computers and Security, 2018, 78, 267-280.	6.0	9
45	Hiding Intermittent Information Leakage with Architectural Support for Blinking. , 2018, , .		9
46	A swarm of autonomous miniature underwater robot drifters for exploring submesoscale ocean dynamics. Nature Communications, 2017, 8, 14189.	12.8	137
47	Arbitrary Precision and Complexity Tradeoffs for Gate-Level Information Flow Tracking. , 2017, , .		4
48	Register transfer level information flow tracking for provably secure hardware design. , 2017, , .		62
49	An Architecture for Learning Stream Distributions with Application to RNG Testing. , 2017, , .		4
50	Radio receiver design for Unmanned Aerial wildlife tracking. , 2017, , .		5
51	A streaming clustering approach using a heterogeneous system for big data analysis. , 2017, , .		4
52	Clepsydra: Modeling timing flows in hardware designs. , 2017, , .		16
53	A message from the general chair and program chair. , 2017, , .		0
54	Why you should care about don't cares: Exploiting internal don't care conditions for hardware Trojans. , 2017, , .		11

#	Article	IF	Citations
55	Rapid design and manufacturing of task-specific autonomous paragliders using 3D printing. , 2017, , .		0
56	Identifying and Measuring Security Critical Path for Uncovering Circuit Vulnerabilities. , 2017, , .		7
57	Imprecise security. , 2016, , .		10
58	Autonomous acoustic trigger for distributed underwater visual monitoring systems. , 2016, , .		1
59	Inter-node distance estimation from ambient acoustic noise in mobile underwater sensor arrays. , 2016, , .		0
60	Towards Property Driven Hardware Security. , 2016, , .		18
61	Ambient noise correlations on a mobile, deformable array. Journal of the Acoustical Society of America, 2016, 140, 4260-4270.	1.1	8
62	Spector: An OpenCL FPGA benchmark suite. , 2016, , .		39
63	Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler. , 2016, , .		1
64	Detecting Hardware Trojans with Gate-Level Information-Flow Tracking. Computer, 2016, 49, 44-52.	1.1	70
65	Detection and time-of-arrival estimation of underwater acoustic signals. , 2016, , .		1
66	Rapid design and manufacturing of task-specific autonomous paragliders using 3D printing. , 2016, , .		1
67	Design of a low-cost and extensible acoustically-triggered camera system for marine population monitoring. , 2016, , .		1
68	Tunnel Vision. Advances in Archaeological Practice, 2016, 4, 192-204.	1.2	6
69	A Brainâ€“Computer Interface (BCI) for the Detection of Mine-Like Objects in Sidescan Sonar Imagery. IEEE Journal of Oceanic Engineering, 2016, 41, 123-138.	3.8	39
70	Hardware Accelerated Alignment Algorithm for Optical Labeled Genomes. ACM Transactions on Reconfigurable Technology and Systems, 2016, 9, 1-21.	2.5	2
71	Resolve. , 2016, , .		17
72	Adaptive Threshold Non-Pareto Elimination: Re-thinking Machine Learning for System Level Design Space Exploration on FPGAs. , 2016, , .		18

#	Article	IF	Citations
73	Composable, Parameterizable Templates for High-Level Synthesis. , 2016, , .		4
74	Quantifying Hardware Security Using Joint Information Flow Analysis. , 2016, , .		0
75	Quantifying timing-based information flow in cryptographic hardware. , 2015, , .		9
76	Scaling the Annotation of Subtidal Marine Habitats. , 2015, , .		8
77	RIFFA 2.1. ACM Transactions on Reconfigurable Technology and Systems, 2015, 8, 1-23.	2.5	99
78	Semisynthetic Versus Real-World Sonar Training Data for the Classification of Mine-Like Objects. IEEE Journal of Oceanic Engineering, 2015, 40, 48-56.	3.8	27
79	Real-time collaborative tracking for underwater networked systems. Ad Hoc Networks, 2015, 34, 196-210.	5.5	19
80	A scalable FPGA architecture for nonnegative least squares problems. , 2015, , .		2
81	ToA-TS: Time of arrival based joint time synchronization and tracking for mobile underwater systems. Ad Hoc Networks, 2015, 34, 211-223.	5.5	75
82	Small Unmanned Aerial Vehicle System for Wildlife Radio Collar Tracking. , 2014, , .		24
83	Improving FPGA accelerated tracking with multiple online trained classifiers. , 2014, , .		2
84	Real-time 3D reconstruction for FPGAs: A case study for evaluating the performance, area, and programmability trade-offs of the Altera OpenCL SDK. , 2014, , .		13
85	Gate-Level Information Flow Tracking for Security Lattices. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-25.	2.6	29
86	Leveraging Gate-Level Properties to Identify Hardware Timing Channels. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1288-1301.	2.7	39
87	High throughput channel tracking for JTRS wireless channel emulation. , 2014, , .		3
88	Hardware accelerated novel optical de novo assembly for large-scale genomes. , 2014, , .		7
89	Energy efficient canonical huffman encoding. , 2014, , .		8
90	FPGA Accelerated Online Boosting for Multi-target Tracking. , 2014, , .		3

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91	Sapper. , 2014, , .		83
92	Networks on Chip with Provable Security Properties. IEEE Micro, 2014, 34, 57-68.	1.8	31
93	Sapper. Computer Architecture News, 2014, 42, 97-112.	2.5	12
94	Sapper. ACM SIGPLAN Notices, 2014, 49, 97-112.	0.2	4
95	Expanding Gate Level Information Flow Tracking for Multilevel Security. IEEE Embedded Systems Letters, 2013, 5, 25-28.	1.9	14
96	Simplified p-norm-like constraint LMS algorithm for efficient estimation of underwater acoustic channels. Journal of Marine Science and Application, 2013, 12, 228-234.	1.7	9
97	A hardware accelerated approach for imaging flow cytometry. , 2013, , .		3
98	Eliminating Timing Information Flows in a Mix-Trusted System-on-Chip. IEEE Design and Test, 2013, 30, 55-62.	1.2	12
99	A 3-D Split Manufacturing Approach to Trustworthy System Development. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 611-615.	2.7	53
100	A software-based dynamic-warp scheduling approach for load-balancing the Violaâ€“Jones face detection algorithm on GPUs. Journal of Parallel and Distributed Computing, 2013, 73, 677-685.	4.1	9
101	Energy efficient signaling strategies for tracking mobile underwater vehicles. , 2013, , .		4
102	RIFFA 2.0: A reusable integration framework for FPGA accelerators. , 2013, , .		34
103	SurfNoC. , 2013, , .		68
104	Position paper. , 2013, , .		1
105	A low-power Adaboost-based object detection processor using Haar-like features. , 2013, , .		10
106	A FPGA design for high speed feature extraction from a compressed measurement stream. , 2013, , .		0
107	A Practical Testing Framework for Isolating Hardware Timing Channels. , 2013, , .		11
108	Joint time synchronization and tracking for mobile underwater systems. , 2013, , .		5

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109	SurfNoC. Computer Architecture News, 2013, 41, 583-594.	2.5	33
110	Circuit Primitives for Monitoring Information Flow and Enabling Redundancy. Lecture Notes in Computer Science, 2013, , 6-6.	1.3	1
111	Design of a Reconfigurable Acoustic Modem for Underwater Sensor Networks. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 821-823.	0.3	0
112	Simultaneous information flow security and circuit redundancy in Boolean gates. , 2012, , .		7
113	Real-time collaborative tracking for underwater networked systems. , 2012, , .		9
114	GPU acceleration of optical mapping algorithm for cardiac electrophysiology. , 2012, 2012, 1558-61.		1
115	Sensor platforms for multimodal underwater monitoring. , 2012, , .		10
116	Designing a hardware in the loop wireless digital channel emulator for software defined radio. , 2012, , .		22
117	FPGA-GPU-CPU heterogenous architecture for real-time cardiac physiological optical mapping. , 2012, , .		19
118	RIFFA: A Reusable Integration Framework for FPGA Accelerators. , 2012, , .		22
119	Designing an Adaptive Acoustic Modem for Underwater Sensor Networks. IEEE Embedded Systems Letters, 2012, 4, 1-4.	1.9	35
120	On the Complexity of Generating Gate Level Information Flow Tracking Logic. IEEE Transactions on Information Forensics and Security, 2012, 7, 1067-1080.	6.9	28
121	A Qualitative Security Analysis of a New Class of 3-D Integrated Crypto Co-processors. Lecture Notes in Computer Science, 2012, , 364-382.	1.3	13
122	Determining the Suitability of FPGAs for a Low-Cost, Low-Power Underwater Acoustic Modem. Lecture Notes in Electrical Engineering, 2012, , 509-517.	0.4	2
123	Design and Implementation of an FPGA-Based Real-Time Face Recognition System. , 2011, , .		32
124	Theoretical Fundamentals of Gate Level Information Flow Tracking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1128-1140.	2.7	49
125	Simulate and Eliminate: A Top-to-Bottom Design Methodology for Automatic Generation of Application Specific Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1173-1183.	2.7	8
126	The stingray AUV: A small and cost-effective solution for ecological monitoring. , 2011, , .		4

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127	Integrating Embedded Computing Systems Into High School and Early Undergraduate Education. IEEE Transactions on Education, 2011, 54, 197-202.	2.4	11
128	Guest Editorial Special Section on Embedded Reconfigurable Computing Systems. IEEE Embedded Systems Letters, 2011, 3, 75-76.	1.9	0
129	Information flow isolation in I2C and USB. , 2011, , .		47
130	Crafting a usable microkernel, processor, and I/O system with strict and provable information flow security. , 2011, , .		78
131	Strategies for Implementing Hardware-Assisted High-Throughput Cellular Image Analysis. Journal of the Association for Laboratory Automation, 2011, 16, 422-430.	2.8	17
132	Crafting a usable microkernel, processor, and I/O system with strict and provable information flow security. Computer Architecture News, 2011, 39, 189-200.	2.5	10
133	JBoost Optimization of Color Detectors for Autonomous Underwater Vehicle Navigation. Lecture Notes in Computer Science, 2011, , 155-162.	1.3	3
134	Theoretical analysis of gate level information flow tracking. , 2010, , .		25
135	Layout Aware Optimization of High Speed Fixed Coefficient FIR Filters for FPGAs. International Journal of Reconfigurable Computing, 2010, 2010, 1-17.	0.2	19
136	Channel Equalization Based on Data Reuse LMS Algorithm for Shallow Water Acoustic Communication. , 2010, , .		6
137	GUSTO. Transactions on Embedded Computing Systems, 2010, 9, 1-21.	2.9	23
138	Hardware assistance for trustworthy systems through 3-D integration. , 2010, , .		12
139	R&D of a dual mode acoustic modem testbed for shallow water channels. , 2010, , .		2
140	Hardware Implementation of Symbol Synchronization for Underwater FSK. , 2010, , .		10
141	Increased Performace of FPGA-Based Color Classification System. , 2010, , .		5
142	Security Primitives for Reconfigurable Hardware-Based Systems. ACM Transactions on Reconfigurable Technology and Systems, 2010, 3, 1-35.	2.5	11
143	Accelerating Viola-Jones Face Detection to FPGA-Level Using GPUs. , 2010, , .		74
144	Design of a Low-Cost Underwater Acoustic Modem. IEEE Embedded Systems Letters, 2010, 2, 58-61.	1.9	57

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145	Handbook of FPGA Design Security. , 2010, , .		33
146	Field Programmable Gate Array Implementation of Parts-Based Object Detection for Real Time Video Applications. , 2010, , .		6
147	Hardware trust implications of 3-D integration. , 2010, , .		6
148	Spatial Separation with Moats. , 2010, , 127-138.		0
149	Hardware Security Challenges. , 2010, , 71-85.		0
150	FPGA Updates and Programmability. , 2010, , 87-96.		0
151	Memory Protection on FPGAs. , 2010, , 97-126.		0
152	Energy benefits of reconfigurable hardware for use in underwater snesor nets. , 2009, , .		6
153	Fpga-based face detection system using Haar classifiers. , 2009, , .		111
154	Hardware acceleration of multi-view face detection. , 2009, , .		4
155	Architectural Optimization of Decomposition Algorithms for Wireless Communication Systems. , 2009, , .		2
156	Integrating embedded computing systems into high school and early undergraduate education. , 2009, , .		0
157	Parallelized Architecture of Multiple Classifiers for Face Detection. , 2009, , .		37
158	Enforcing memory policy specifications in reconfigurable hardware. Computers and Security, 2008, 27, 197-215.	6.0	22
159	Managing Security in FPGA-Based Embedded Systems. IEEE Design and Test of Computers, 2008, 25, 590-598.	1.0	44
160	Automatic generation of decomposition based matrix inversion architectures. , 2008, , .		10
161	Extended abstract: Trustworthy system security through 3-D integrated hardware. , 2008, , .		4
162	Design space exploration of a cooperative MIMO receiver for reconfigurable architectures. , 2008, , .		3

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163	An FPGA Design Space Exploration Tool for Matrix Inversion Architectures. , 2008, , .		20
164	Designing secure systems on reconfigurable hardware. ACM Transactions on Design Automation of Electronic Systems, 2008, 13, 1-24.	2.6	22
165	FPGA acceleration of mean variance framework for optimal asset allocation. , 2008, , .		7
166	Operation Scheduling: Algorithms and Applications. , 2008, , 231-255.		7
167	Survey of hardware platforms for an energy efficient implementation of matching pursuits algorithm for shallow water networks. , 2008, , .		6
168	Exploring time/resource trade-offs by solving dual scheduling problems with the ant colony optimization. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 46.	2.6	11
169	Ant Colony Optimizations for Resource- and Timing-Constrained Operation Scheduling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1010-1029.	2.7	33
170	Combining static and dynamic defect-tolerance techniques for nanoscale memory systems. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	2
171	Moats and Drawbridges: An Isolation Primitive for Reconfigurable Hardware Based Systems. , 2007, , .		71
172	A pageable, defect-tolerant nanoscale memory system. , 2007, , .		8
173	Implementation of the Alamouti OSTBC to a Distributed Set of Single-Antenna Wireless Nodes. , 2007, , .		3
174	Algebraic Methods for Optimizing Constant Multiplications in Linear Systems. Journal of Signal Processing Systems, 2007, 49, 31-50.	1.0	6
175	FPGA Implementation of High Speed FIR Filters Using Add and Shift Method. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	55
176	Leakage power reduction of embedded memories on FPGAs through location assignment. , 2006, , .		10
177	Design space exploration using time and resource duality with the ant colony optimization. , 2006, , .		17
178	Design of a low-cost acoustic modem for moored oceanographic applications. , 2006, , .		35
179	Defect-Tolerant Nanocomputing Using Bloom Filters. , 2006, , .		2
180	On the Use of Bloom Filters for Defect Maps in Nanocomputing. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	3

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181	Design and Development of a Software-Defined Underwater Acoustic Modem for Sensor Networks for Environmental and Ecological Research. , 2006, , .		20
182	GEN05-4: Carrier Offset and Channel Estimation for Cooperative MIMO Sensor Networks. IEEE Global Telecommunications Conference (GLOBECOM), 2006, , .	0.0	10
183	Policy-Driven Memory Protection for Reconfigurable Hardware. Lecture Notes in Computer Science, 2006, , 461-478.	1.3	18
184	MP core. , 2005, , .		19
185	Instruction scheduling using MAX-MIN ant system optimization. , 2005, , .		6
186	Algorithm/Architecture Co-exploration for Designing Energy Efficient Wireless Channel Estimator. Journal of Low Power Electronics, 2005, 1, 238-248.	0.6	17
187	Title is missing!. Design Automation for Embedded Systems, 2000, 5, 329-338.	1.0	21