Jaehyeong Sim

List of Publications by Year
in descending order

19 papers	316 citations	1478505 6 h-index	1720034 7 g-index
19 all docs	19 docs citations	19 times ranked	383 citing authors

#	Article	IF	Citations
1	S-FLASH: A NAND Flash-based Deep Neural Network Accelerator Exploiting Bit-level Sparsity. IEEE Transactions on Computers, 2021, , 1-1.	3.4	10
2	An Energy-Efficient Deep Convolutional Neural Network Inference Processor With Enhanced Output Stationary Dataflow in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 87-100.	3.1	40
3	An Energy-Efficient Deep Convolutional Neural Network Training Accelerator for In Situ Personalization on Smart Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2691-2702.	5.4	32
4	CREMON: Cryptography Embedded on the Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3337-3341.	3.0	6
5	NAND-Net: Minimizing Computational Complexity of In-Memory Processing for Binary Neural Networks. , 2019, , .		25
6	A 47.4ÂµJ/epoch Trainable Deep Convolutional Neural Network Accelerator for In-Situ Personalization on Smart Devices. , 2019, , .		2
7	eSRCNN: A Framework for Optimizing Super-Resolution Tasks on Diverse Embedded CNN Accelerators. , 2019, , .		4
8	An Energy-efficient Processing-in-memory Architecture for Long Short Term Memory in Spin Orbit Torque MRAM. , 2019, , .		4
9	A PVT-robust Customized 4T Embedded DRAM Cell Array for Accelerating Binary Neural Networks. , 2019, , .		5
10	NID. , 2018, , .		11
11	TrainWare. , 2018, , .		13
12	Energy-Efficient Design of Processing Element for Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1332-1336.	3.0	25
13	A Kernel Decomposition Architecture for Binary-weight Convolutional Neural Networks. , 2017, , .		25
14	SENIN: An energy-efficient sparse neuromorphic system with on-chip learning. , 2017, , .		3
15	14.6 A 1.42TOPS/W deep convolutional neural network recognition processor for intelligent IoE systems. , 2016, , .		94
16	A 5-Gb/s 2.67-mW/Gb/s Digital Clock and Data Recovery With Hybrid Dithering Using a Time-Dithered Deltaâ€“Sigma Modulator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1450-1459.	3.1	9
17	Timing error masking by exploiting operand value locality in SIMD architecture. , 2014, , .		0
18	PowerField: A Probabilistic Approach for Temperature-to-Power Conversion Based on Markov Random Field Theory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1509-1519.	2.7	6

#	Article	IF	Citations
19	PowerField. , 2012, , .		2