

Jaehyeong Sim

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	14.6 A 1.42TOPS/W deep convolutional neural network recognition processor for intelligent IoT systems. , 2016, , .		94
2	An Energy-Efficient Deep Convolutional Neural Network Inference Processor With Enhanced Output Stationary Dataflow in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 87-100.	3.1	40
3	An Energy-Efficient Deep Convolutional Neural Network Training Accelerator for <i>In Situ</i> Personalization on Smart Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2691-2702.	5.4	32
4	Energy-Efficient Design of Processing Element for Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1332-1336.	3.0	25
5	A Kernel Decomposition Architecture for Binary-weight Convolutional Neural Networks. , 2017, , .		25
6	NAND-Net: Minimizing Computational Complexity of In-Memory Processing for Binary Neural Networks. , 2019, , .		25
7	TrainWare. , 2018, , .		13
8	NID. , 2018, , .		11
9	S-FLASH: A NAND Flash-based Deep Neural Network Accelerator Exploiting Bit-level Sparsity. IEEE Transactions on Computers, 2021, , 1-1.	3.4	10
10	A 5-Gb/s 2.67-mW/Gb/s Digital Clock and Data Recovery With Hybrid Dithering Using a Time-Dithered Delta- Σ Modulator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1450-1459.	3.1	9
11	PowerField: A Probabilistic Approach for Temperature-to-Power Conversion Based on Markov Random Field Theory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1509-1519.	2.7	6
12	CREMON: Cryptography Embedded on the Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3337-3341.	3.0	6
13	A PVT-robust Customized 4T Embedded DRAM Cell Array for Accelerating Binary Neural Networks. , 2019, , .		5
14	eSRCNN: A Framework for Optimizing Super-Resolution Tasks on Diverse Embedded CNN Accelerators. , 2019, , .		4
15	An Energy-efficient Processing-in-memory Architecture for Long Short Term Memory in Spin Orbit Torque MRAM. , 2019, , .		4
16	SENIN: An energy-efficient sparse neuromorphic system with on-chip learning. , 2017, , .		3
17	PowerField. , 2012, , .		2
18	A 47.4 μ /epoch Trainable Deep Convolutional Neural Network Accelerator for In-Situ Personalization on Smart Devices. , 2019, , .		2

#	ARTICLE	IF	CITATIONS
19	Timing error masking by exploiting operand value locality in SIMD architecture. , 2014, , .		0