Sherief Reda

List of Publications by Year
in descending order

76 papers	1,648 citations	516710 16 h-index	580821 25 g-index
76 all docs	76 docs citations	76 times ranked	1230 citing authors

#	Article	IF	Citations
1	CasCon: Cascaded Thermal and Electrical Current Throttling for Mobile Devices. IEEE Embedded Systems Letters, 2022, 14, 3-6.	1.9	0
2	Approximate Logic Synthesis Using Boolean Matrix Factorization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 15-28.	2.7	7
3	PACT: An Extensible Parallel Thermal Simulator for Emerging Integration and Cooling Technologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1048-1061.	2.7	7
4	Characterizing and Optimizing EDA Flows for the Cloud. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3040-3051.	2.7	5
5	Coordinated Batching and DVFS for DNN Inference on GPU Accelerators. IEEE Transactions on Parallel and Distributed Systems, 2022, 33, 2496-2508.	5.6	21
6	ISLPED 2021: The 25th Anniversary!. IEEE Design and Test, 2022, 39, 92-93.	1.2	0
7	Alternating Blind Identification of Power Sources for Mobile SoCs. , 2022, , .		0
8	ARBench: Augmented Reality Benchmark For Mobile Devices. , 2022, , .		3
9	Leveraging autocatalytic reactions for chemical domain image classification. Chemical Science, 2021, 12, 5464-5472.	7.4	4
10	Implementing parallel arithmetic via acetylation and its application to chemical image processing. Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences, 2021, 477, .	2.1	1
11	Guest Editorsâ€™ Introduction: The Resurgence of Open-Source EDA Technology. IEEE Design and Test, 2021, 38, 5-7.	1.2	0
12	BatchSizer. , 2021, , .		7
13	BayesTuner: Leveraging Bayesian Optimization For DNN Inference Configuration Selection. IEEE Computer Architecture Letters, 2021, 20, 166-170.	1.5	1
14	AdaCon: Adaptive Context-Aware Object Detection for Resource-Constrained Embedded Devices. , 2021, , .		1
15	LoCool: Fighting Hot Spots Locally for Improving System Energy Efficiency. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 895-908.	2.7	9
16	PowerCoord: Power capping coordination for multi-CPU/GPU servers using reinforcement learning. Sustainable Computing: Informatics and Systems, 2020, 28, 100412.	2.2	3
17	ApproxDNN: Incentivizing DNN Approximation in Cloud. , 2020, , .		3
18	AdaSense: Adaptive Low-Power Sensing and Activity Recognition for Wearable Devices. , 2020, , .		1

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19	Approximate Logic Synthesis: A Survey. Proceedings of the IEEE, 2020, 108, 2195-2213.	21.3	54
20	A Learning-Based Thermal Simulation Framework for Emerging Two-Phase Cooling Technologies. , 2020, , .		1
21	Coordinated Self-Tuning Thermal Management Controller for Mobile Devices. IEEE Design and Test, 2020, 37, 34-41.	1.2	4
22	Principles of Information Storage in Small-Molecule Mixtures. IEEE Transactions on Nanobioscience, 2020, 19, 378-384.	3.3	17
23	DRiLLS: Deep Reinforcement Learning for Logic Synthesis. , 2020, , .		47
24	Dual-precision fixed-point arithmetic for low-power ray-triangle intersections. Computers and Graphics, 2020, 87, 72-79.	2.5	3
25	Multicomponent molecular memory. Nature Communications, 2020, 11, 691.	12.8	40
26	Temperature and Supply Voltage Monitoring with Current-mode Relaxation Oscillators. , 2020, , .		1
27	Two-Phase Vapor Chambers with Micropillar Evaporators: A New Approach to Remove Heat from Future High-Performance Chips. , 2019, , .		3
28	Toward an Open-Source Digital Flow. , 2019, , .		81
29	Modeling and Optimization of Chip Cooling with Two-Phase Vapor Chambers. , 2019, , .		4
30	Generalized Matrix Factorization Techniques for Approximate Logic Synthesis. , 2019, , .		4
31	Coordinated DVFS and Precision Control for Deep Neural Networks. IEEE Computer Architecture Letters, 2019, 18, 136-140.	1.5	17
32	Automated High-Level Generation of Low-Power Approximate Computing Circuits. IEEE Transactions on Emerging Topics in Computing, 2019, 7, 18-30.	4.6	47
33	Blind Identification of Thermal Models and Power Sources From Thermal Measurements. IEEE Sensors Journal, 2018, 18, 680-691.	4.7	16
34	Approximate Computing for Biometric Security Systems: A Case Study on Iris Scanning. , 2018, , .		13
35	PowerCoord: A Coordinated Power Capping Controller for Multi-CPU/GPU Servers. , 2018, , .		8
36	Understanding the Sources of Power Consumption in Mobile SoCs. , 2018, , .		3

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37	Parallelized Linear Classification with Volumetric Chemical Perceptrons. , 2018, , .		7
38	BLASYS: Approximate Logic Synthesis Using Boolean Matrix Factorization. , 2018, , .		8
39	Computing with Chemicals: Perceptrons Using Mixtures of Small Molecules. , 2018, , .		2
40	QoR-aware power capping for approximate big data processing. , 2018, , .		0
41	BLASYS. , 2018, , .		34
42	Hardware-Software Codesign of Accurate, Multiplier-free Deep Neural Networks. , 2017, , .		46
43	Blind identification of power sources in processors. , 2017, , .		4
44	Understanding the impact of precision quantization on the accuracy and energy of neural networks. , 2017, , .		60
45	3D integration advances computing. Nature, 2017, 547, 38-39.	27.8	12
46	Scheduling on CPU + GPU Processors Under Dynamic Conditions. Journal of Low Power Electronics, 2017, 13, 551-568.	0.6	0
47	Creating Soft Heterogeneity in Clusters Through Firmware Re-configuration. , 2016, , .		0
48	A low-power dynamic divider for approximate applications. , 2016, , .		39
49	Power-aware characterization and mapping of workloads on CPU-GPU processors. , 2016, , .		7
50	Scheduling Challenges and Opportunities in Integrated CPU+GPU Processors. , 2016, , .		13
51	DRUM: A Dynamic Range Unbiased Multiplier for approximate applications. , 2015, , .		211
52	How Good Are Low-Power 64-Bit SoCs for Server-Class Workloads?. , 2015, , .		8
53	Power Budgeting Techniques for Data Centers. IEEE Transactions on Computers, 2015, 64, 2267-2278.	3.4	20
54	Novel Techniques for High-Sensitivity Hardware Trojan Detection Using Thermal and Power Maps. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1792-1805.	2.7	97

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55	ABACUS: A technique for automated behavioral synthesis of approximate computing circuits. , 2014, , .		18
56	ABACUS: A technique for automated behavioral synthesis of approximate computing circuits. , 2014, , .		36
57	Power Mapping of Integrated Circuits Using AC-Based Thermography. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1398-1409.	3.1	9
58	Mitigating Dark Silicon Problems Using Superlattice-based Thermoelectric Coolers. , 2013, , .		8
59	High-Sensitivity Hardware Trojan Detection Using Multimodal Characterization. , 2013, , .		41
60	Power mapping and modeling of multi-core processors. , 2013, , .		23
61	Thermal prediction and adaptive control through workload phase detection. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-19.	2.6	21
62	Adaptive Power Capping for Servers with Multithreaded Workloads. IEEE Micro, 2012, 32, 64-75.	1.8	41
63	Fast Multi-Objective Algorithmic Design Co-Exploration for FPGA-based Accelerators. , 2012, , .		4
64	Power Modeling and Characterization of Computing Devices. Foundations and Trends in Electronic Design Automation, 2012, 6, 121-216.	1.0	25
65	Identifying the optimal energy-efficient operating points of parallel workloads. , 2011, , .		20
66	Thermal and Power Characterization of Real Computing Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 76-87.	3.6	22
67	Improved Thermal Tracking for Processors Using Hard and Soft Sensor Allocation Techniques. IEEE Transactions on Computers, 2011, 60, 841-851.	3.4	66
68	Pack & Cap. , 2011, , .		198
69	Early estimation of TSV area for power delivery in 3-D integrated circuits. , 2010, , .		3
70	Accurate Spatial Estimation and Decomposition Techniques for Variability Characterization. IEEE Transactions on Semiconductor Manufacturing, 2010, 23, 345-357.	1.7	15
71	Analyzing the impact of process variations on parametric measurements: Novel models and applications. , 2009, , .		26
72	Frequency and voltage planning for multi-core processors under thermal constraints. , 2008, , .		16

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73	On-Line Adjustable Buffering for Runtime Power Reduction. , 2007, , .		3
74	Strategies for improving the parametric yield and profits of 3D ICs. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	16
75	Scalable Heuristics for Design of DNA Probe Arrays. Journal of Computational Biology, 2004, 11, 429-447.	1.6	10
76	Match twice and stitch: a new TSP tour construction heuristic. Operations Research Letters, 2004, 32, 499-509.	0.7	23