Nasir Shaikh-Husin

List of Publications by Year
in descending order

16	112	1684188 5	1872680 6
papers	citations	h-index	g-index

16	16	16	84
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Accurate and compact convolutional neural network based on stochastic computing. Neurocomputing, 2022, 471, 31-47.	5.9	20
2	CNTFET based Voltage Mode MISO Active only Biquadratic Filter for Multi-GHz Frequency Applications. Circuits, Systems, and Signal Processing, 2021, 40, 4721-4740.	2.0	6
3	Low-area and accurate inner product and digital filters based on stochastic computing. Signal Processing, 2021, 183, 108040.	3.7	10
4	Characterization of Correlation in Stochastic Computing Functions. , 2020, , .		0
5	Accurate and compact stochastic computations by exploiting correlation. Turkish Journal of Electrical Engineering and Computer Sciences, 2019, 27, 547-564.	1.4	11
6	A linked list run-length-based single-pass connected component analysis for real-time embedded hardware. Journal of Real-Time Image Processing, 2018, 15, 197-215.	3.5	21
7	An optimized buffer insertion algorithm with delay-power constraints for VLSI layouts. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 844-861.	1.4	0
8	FPGA-Based Real-Time Moving Target Detection System for Unmanned Aerial Vehicle Application. International Journal of Reconfigurable Computing, 2016, 2016, 1-16.	0.2	19
9	DYNAMIC POWER DISSIPATION FORMULATION FOR APPLICATION IN DYNAMIC PROGRAMMING BUFFER INSERTION ALGORITHM. Jurnal Teknologi (Sciences and Engineering), 2016, 78, .	0.4	0
10	Hardware acceleration of a face detection system on FPGA. , 2015, , .		5
11	Algorithm to convert programmable logic controller Ladder Logic Diagram models to Petri Net models. , 2015, , .		3
12	Low cost pipelined FPGA architecture of Harris Corner Detector for real-time applications. , 2015, , .		5
13	FPGA implementation of RANSAC algorithm for real-time image geometry estimation. , 2013, , .		6
14	Feasible transition path generation for EFSM-based system testing. , 2013, , .		4
15	Deadlock detection and avoidance using Signal Interpreted Petri Nets. , 2012, , .		1
16	Simultaneous Routing and Buffer Insertion algorithm for interconnect delay optimization in VLSI layout design. , 2008, , .		1