

Nasir Shaikh-Husin

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/1492503/publications.pdf>

Version: 2024-02-01

16
papers

112
citations

1684188

5
h-index

1872680

6
g-index

16
all docs

16
docs citations

16
times ranked

84
citing authors

#	ARTICLE	IF	CITATIONS
1	A linked list run-length-based single-pass connected component analysis for real-time embedded hardware. <i>Journal of Real-Time Image Processing</i> , 2018, 15, 197-215.	3.5	21
2	Accurate and compact convolutional neural network based on stochastic computing. <i>Neurocomputing</i> , 2022, 471, 31-47.	5.9	20
3	FPGA-Based Real-Time Moving Target Detection System for Unmanned Aerial Vehicle Application. <i>International Journal of Reconfigurable Computing</i> , 2016, 2016, 1-16.	0.2	19
4	Accurate and compact stochastic computations by exploiting correlation. <i>Turkish Journal of Electrical Engineering and Computer Sciences</i> , 2019, 27, 547-564.	1.4	11
5	Low-area and accurate inner product and digital filters based on stochastic computing. <i>Signal Processing</i> , 2021, 183, 108040.	3.7	10
6	FPGA implementation of RANSAC algorithm for real-time image geometry estimation. , 2013, , .		6
7	CNTFET based Voltage Mode MISO Active only Biquadratic Filter for Multi-GHz Frequency Applications. <i>Circuits, Systems, and Signal Processing</i> , 2021, 40, 4721-4740.	2.0	6
8	Hardware acceleration of a face detection system on FPGA. , 2015, , .		5
9	Low cost pipelined FPGA architecture of Harris Corner Detector for real-time applications. , 2015, , .		5
10	Feasible transition path generation for EFSM-based system testing. , 2013, , .		4
11	Algorithm to convert programmable logic controller Ladder Logic Diagram models to Petri Net models. , 2015, , .		3
12	Simultaneous Routing and Buffer Insertion algorithm for interconnect delay optimization in VLSI layout design. , 2008, , .		1
13	Deadlock detection and avoidance using Signal Interpreted Petri Nets. , 2012, , .		1
14	An optimized buffer insertion algorithm with delay-power constraints for VLSI layouts. <i>Turkish Journal of Electrical Engineering and Computer Sciences</i> , 2017, 25, 844-861.	1.4	0
15	Characterization of Correlation in Stochastic Computing Functions. , 2020, , .		0
16	DYNAMIC POWER DISSIPATION FORMULATION FOR APPLICATION IN DYNAMIC PROGRAMMING BUFFER INSERTION ALGORITHM. <i>Jurnal Teknologi (Sciences and Engineering)</i> , 2016, 78, .	0.4	0