Ramesh Karri

List of Publications by Year
in descending order

263 papers	7,900 citations	117625 34 h-index	98798 67 g-index
271 all docs	271 docs citations	271 times ranked	3226 citing authors

#	Article	IF	Citations
1	A Primer on Hardware Security: Models, Methods, and Metrics. Proceedings of the IEEE, 2014, 102, 1283-1295.	21.3	471
2	Trustworthy Hardware: Identifying and Classifying Hardware Trojans. Computer, 2010, 43, 39-46.	1.1	403
3	Security analysis of logic obfuscation. , 2012, , .		366
4	Fault Analysis-Based Logic Encryption. IEEE Transactions on Computers, 2015, 64, 410-424.	3.4	352
5	Security analysis of integrated circuit camouflaging. , 2013, , .		287
6	The Cybersecurity Landscape in Industrial Control Systems. Proceedings of the IEEE, 2016, 104, 1039-1057.	21.3	249
7	On Improving the Security of Logic Locking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1411-1424.	2.7	232
8	On design vulnerability analysis and trust benchmarks development. , 2013, , .		183
9	The Robust QCA Adder Designs Using Composable QCA Building Blocks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 176-183.	2.7	180
10	Manufacturing and Security Challenges in 3D Printing. Jom, 2016, 68, 1872-1881.	1.9	172
11	Is Split Manufacturing Secure?. , 2013, , .		140
12	Attacks and Defenses for JTAG. IEEE Design and Test of Computers, 2010, 27, 36-47.	1.0	115
13	Leveraging Memristive Systems in the Construction of Digital Logic Circuits. Proceedings of the IEEE, 2012, 100, 2033-2049.	21.3	103
14	Nano Meets Security: Exploring Nanoelectronic Devices for Security Applications. Proceedings of the IEEE, 2015, 103, 829-849.	21.3	102
15	Sneak-Path Testing of Crossbar-Based Nonvolatile Random Access Memories. IEEE Nanotechnology Magazine, 2013, 12, 413-426.	2.0	101
16	Hardware and embedded security in the context of internet of things. , 2013, , .		85
17	Low cost concurrent error detection for the advanced encryption standard. , 0, , .		84
18	Cybersecurity of Smart Electric Vehicle Charging: A Power Grid Perspective. IEEE Access, 2020, 8, 214434-214453.	4.2	84

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19	Trustworthy Hardware: Trojan Detection and Design-for-Trust Challenges. Computer, 2011, 44, 66-74.	1.1	81
20	Are hardware performance counters a cost effective way for integrity checking of programs. , 2011, , .		80
21	Detecting malicious modifications of data in third-party intellectual property cores. , 2015, , .		80
22	An Energy-Efficient Memristive Threshold Logic Circuit. IEEE Transactions on Computers, 2012, 61, 474-487.	3.4	79
23	Nano-PPUF: A Memristor-Based Security Primitive. , 2012, , .		78
24	NumChecker. , 2013, , .		77
25	Cybersecurity for Control Systems: A Process-Aware Perspective. IEEE Design and Test, 2016, 33, 75-83.	1.2	72
26	Public Plug-in Electric Vehicles + Grid Data: Is a New Cyberattack Vector Viable?. IEEE Transactions on Smart Grid, 2020, 11, 5099-5113.	9.0	72
27	Regaining Trust in VLSI Design: Design-for-Trust Techniques. Proceedings of the IEEE, 2014, 102, 1266-1282.	21.3	68
28	Additive Manufacturing Cyber-Physical System: Supply Chain Cybersecurity and Risks. IEEE Access, 2020, 8, 47322-47333.	4.2	68
29	Sensor physical unclonable functions. , 2010, , .		64
30	Securing Hardware Accelerators: A New Challenge for High-Level Synthesis. IEEE Embedded Systems Letters, 2018, 10, 77-80.	1.9	63
31	Modeling, Detection, and Diagnosis of Faults in Multilevel Memristor Memories. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 822-834.	2.7	61
32	Security analysis of concurrent error detection against differential fault analysis. Journal of Cryptographic Engineering, 2015, 5, 153-169.	1.8	61
33	Building Trustworthy Systems Using Untrusted Components: A High-Level Synthesis Approach. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2946-2959.	3.1	60
34	Design and analysis of ring oscillator based Design-for-Trust technique. , 2011, , .		58
35	Reusing Hardware Performance Counters to Detect and Identify Kernel Control-Flow Modifying Rootkits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 485-498.	2.7	57
36	Automatic synthesis of self-recovering VLSI systems. IEEE Transactions on Computers, 1996, 45, 131-142.	3.4	55

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37	ConFirm: Detecting firmware modifications in embedded systems using Hardware Performance Counters. , 2015, , .		55
38	Recomputing with Permuted Operands: A Concurrent Error Detection Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1595-1608.	2.7	54
39	Security Assessment of Cyberphysical Digital Microfluidic Biochips. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2016, 13, 445-458.	3.0	50
40	Automotive Electrical and Electronic Architecture Security via Distributed In-Vehicle Traffic Monitoring. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1790-1803.	2.7	44
41	Anomaly Detection in Real-Time Multi-Threaded Processes Using Hardware Performance Counters. IEEE Transactions on Information Forensics and Security, 2020, 15, 666-680.	6.9	44
42	Novel Test-Mode-Only Scan Attack and Countermeasure for Compression-Based Scan Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 808-821.	2.7	43
43	Memristor based programmable threshold logic array. , 2010, , .		42
44	Sneak-path Testing of Memristor-based Memories. , 2013, , .		42
45	Secure Randomized Checkpointing for Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1119-1132.	2.7	42
46	Shielding Heterogeneous MPSoCs From Untrustworthy 3PIPs Through Security- Driven Task Scheduling. IEEE Transactions on Emerging Topics in Computing, 2014, 2, 461-472.	4.6	41
47	Formal Security Verification of Third Party Intellectual Property Cores for Information Leakage. , 2016, , .		40
48	Malicious Firmware Detection with Hardware Performance Counters. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 160-173.	2.4	40
49	A Theoretical Study of Hardware Performance Counters-Based Malware Detection. IEEE Transactions on Information Forensics and Security, 2020, 15, 512-525.	6.9	40
50	Hardware Performance Counter-Based Malware Identification and Detection with Adaptive Compressive Sensing. Transactions on Architecture and Code Optimization, 2016, 13, 1-23.	2.0	39
51	Coactive scheduling and checkpoint determination during high level synthesis of self-recovering microarchitectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1994, 2, 304-311.	3.1	38
52	BRAIN: BehavioR Based Adaptive Intrusion Detection in Networks: Using Hardware Performance Counters to Detect DDoS Attacks. , 2016, , .		38
53	Concurrent error detection of fault-based side-channel cryptanalysis of 128-bit symmetric block ciphers. , 2001, , .		37
54	High-level synthesis for security and trust. , 2013, , .		37

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55	Microfluidic encryption of on-chip biochemical assays. , 2016, , .		37
56	Scan-based attacks on linear feedback shift register based stream ciphers. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-15.	2.6	35
57	Security Vulnerabilities of Emerging Nonvolatile Main Memories and Countermeasures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 2-15.	2.7	35
58	ASSURE: RTL Locking Against an Untrusted Foundry. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1306-1318.	3.1	35
59	New scan-based attack using only the test mode. , 2013, , .		34
60	Improving Tolerance to Variations in Memristor-Based Applications Using Parallel Memristors. IEEE Transactions on Computers, 2015, 64, 733-746.	3.4	34
61	VLSI testing based security metric for IC camouflaging. , 2013, , .		33
62	An Approach to Tolerate Process Related Variations in Memristor-Based Applications. , 2011, , .		31
63	TAO. , 2018, , .		31
64	CAD-Base. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-30.	2.6	31
65	Logic Mapping in Crossbar-Based Nanoarchitectures. IEEE Design and Test of Computers, 2009, 26, 68-77.	1.0	30
66	Run-time detection of hardware Trojans: The processor protection unit. , 2013, , .		30
67	Shielding and securing integrated circuits with sensors. , 2014, , .		30
68	Secure scan. , 2005, , .		29
69	Title is missing!. Mobile Networks and Applications, 2003, 8, 177-185.	3.3	28
70	Hardware security strategies exploiting nanoelectronic circuits. , 2013, , .		28
71	Towards Secure Analog Designs: A Secure Sense Amplifier Using Memristors. , 2014, , .		27
72	Process-Aware Covert Channels Using Physical Instrumentation in Cyber-Physical Systems. IEEE Transactions on Information Forensics and Security, 2018, 13, 2761-2771.	6.9	27

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73	Time-constrained scheduling during high-level synthesis of fault-secure VLSI digital signal processors. IEEE Transactions on Reliability, 1996, 45, 404-412.	4.6	26
74	Topology aware mapping of logic functions onto nanowire-based crossbar architectures. , 2006, , .		26
75	Blue team red team approach to hardware trust assessment. , 2011, , .		26
76	TaintHLS: High-Level Synthesis for Dynamic Information Flow Tracking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 798-808.	2.7	26
77	Belling the CAD: Toward Security-Centric Electronic System Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1756-1769.	2.7	25
78	Locking of biochemical assays for digital microfluidic biochips. , 2018, , .		25
79	Securing Processors Against Insider Attacks: A Circuit-Microarchitecture Co-Design Approach. IEEE Design and Test, 2013, 30, 35-44.	1.2	24
80	Detection, diagnosis, and repair of faults in memristor-based memories. , 2014, , .		24
81	Security implications of cyberphysical digital microfluidic biochips. , 2015, , .		23
82	Toward Secure and Trustworthy Cyberphysical Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 589-603.	2.7	23
83	Bio-Protocol Watermarking on Digital Microfluidic Biochips. IEEE Transactions on Information Forensics and Security, 2019, 14, 2901-2915.	6.9	23
84	Introspection. ACM Transactions on Design Automation of Electronic Systems, 2001, 6, 501-515.	2.6	22
85	A Survey of Cybersecurity of Digital Manufacturing. Proceedings of the IEEE, 2021, 109, 495-516.	21.3	22
86	SLICED: Slide-based concurrent error detection technique for symmetric block ciphers. , 2010, , .		21
87	Security-aware SoC test access mechanisms. , 2011, , .		21
88	Invariance-based concurrent error detection for advanced encryption standard. , 2012, , .		20
89	Test-mode-only scan attack using the boundary scan chain. , 2014, , .		20
90	Security Implications of Cyberphysical Flow-Based Microfluidic Biochips. , 2017, , .		20

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91	Hardware Trojan Detection Using the Order of Path Delay. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-23.	2.3	20
92	Trojan Taxonomy. , 2012, , 325-338.		20
93	Test-mode-only scan attack and countermeasure for contemporary scan architectures. , 2014, , .		19
94	Hardware Trojan Detection Using Controlled Circuit Aging. IEEE Access, 2020, 8, 77415-77434.	4.2	19
95	Cyber security threat modeling in the AEC industry: An example for the commissioning of the built environment. Sustainable Cities and Society, 2021, 66, 102682.	10.4	19
96	Sneak path testing and fault modeling for multilevel memristor-based memories. , 2013, , .		18
97	Scan attack in presence of mode-reset countermeasure. , 2013, , .		18
98	Fault Attacks on AES and Their Countermeasures. , 2016, , 163-208.		18
99	Optimal checkpointing for secure intermittently-powered IoT devices. , 2017, , .		18
100	Logic Level Fault Tolerance Approaches Targeting Nanoelectronics PLAs. , 2007, , .		17
101	Securing digital microfluidic biochips by randomizing checkpoints. , 2016, , .		17
102	Emerging (un-)reliability based security threats and mitigations for embedded systems. , 2017, , .		17
103	Execution of provably secure assays on MEDA biochips to thwart attacks. , 2019, , .		17
104	Is Register Transfer Level Locking Secure?. , 2020, , .		17
105	Exploring eFPGA-based Redaction for IP Protection. , 2021, , .		17
106	Fault Tolerant Approaches to Nanoelectronic Programmable Logic Arrays. , 2007, , .		16
107	PREEMPT. , 2019, , .		16
108	Multi-Tenant FPGA-based Reconfigurable Systems: Attacks and Defenses. , 2019, , .		16

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109	Adversarial Perturbation Attacks on ML-based CAD. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-31.	2.6	16
110	Computer aided design of fault-tolerant application specific programmable processors. IEEE Transactions on Computers, 2000, 49, 1272-1284.	3.4	15
111	New scan attacks against state-of-the-art countermeasures and DFT. , 2014, , .		15
112	Opening the Doors to Dynamic Camouflaging: Harnessing the Power of Polymorphic Devices. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 137-156.	4.6	15
113	Towards a New Thermal Monitoring Based Framework for Embedded CPS Device Security. IEEE Transactions on Dependable and Secure Computing, 2022, 19, 524-536.	5.4	15
114	Fortifying RTL Locking Against Oracle-Less (Untrusted Foundry) and Oracle-Guided Attacks. , 2021, , .		15
115	Toward Future Systems with Nanoscale Devices: Overcoming the Reliability Challenge. Computer, 2011, 44, 46-53.	1.1	14
116	Security Trade-Offs in Microfluidic Routing Fabrics. , 2017, , .		14
117	Toward Increasing the Difficulty of Reverse Engineering of RSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-13.	1.7	14
118	Poisoning the (Data) Well in ML-Based CAD: A Case Study of Hiding Lithographic Hotspots. , 2020, , .		14
119	Cyber Insurance Against Cyberattacks on Electric Vehicle Charging Stations. IEEE Transactions on Smart Grid, 2022, 13, 1529-1541.	9.0	14
120	Architecture Support for Dynamic Integrity Checking. IEEE Transactions on Information Forensics and Security, 2012, 7, 321-332.	6.9	13
121	FPGA Trust Zone: Incorporating trust and reliability into FPGA designs. , 2016, , .		13
122	Black-Hat High-Level Synthesis: Myth or Reality?. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 913-926.	3.1	13
123	FLAW3D: A Trojan-Based Cyber Attack on the Physical Outcomes of Additive Manufacturing. IEEE/ASME Transactions on Mechatronics, 2022, 27, 5361-5370.	5.8	13
124	Shielding heterogeneous MPSoCs from untrustworthy 3PIPs through security-driven task scheduling. , 2013, , .		12
125	Security Assessment of Micro-Electrode-Dot-Array Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1831-1843.	2.7	12
126	Toward Secure Microfluidic Fully Programmable Valve Array Biochips. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2755-2766.	3.1	12

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127	TAO: Techniques for Algorithm-Level Obfuscation during High-Level Synthesis. , 2018, , .		11
128	Hardware Trojans Inspired IP Watermarks. IEEE Design and Test, 2019, 36, 72-79.	1.2	11
129	Securing IJTAG against data-integrity attacks. , 2018, , .		10
130	Optimal algorithms for synthesis of reliable application-specific heterogeneous multiprocessors. IEEE Transactions on Reliability, 1995, 44, 603-613.	4.6	9
131	<title>Hardware implementation of a signaling protocol</title>. , 2002, 4874, 174.		9
132	A High-Speed Hardware Architecture for Universal Message Authentication Code. IEEE Journal on Selected Areas in Communications, 2006, 24, 1831-1839.	14.0	9
133	Security challenges during VLSI test. , 2011, , .		9
134	A high-performance, low-overhead microarchitecture for secure program execution. , 2012, , .		9
135	Can the SHIELD protect our integrated circuits?. , 2014, , .		9
136	On enhancing the debug architecture of a system-on-chip (SoC) to detect software attacks. , 2015, , .		9
137	Fingerprinting Field Programmable Gate Arrays. , 2017, , .		9
138	DPFEE: A High Performance Scalable Pre-Processor for Network Security Systems. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 55-68.	2.4	9
139	Desieve the Attacker: Thwarting IP Theft in Sieve-Valve-based Biochips. , 2019, , .		9
140	Exposing Hardware Trojans in Embedded Platforms via Short-Term Aging. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3519-3530.	2.7	9
141	Robust Deep Learning for IC Test Problems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 183-195.	2.7	9
142	HOLL: Program Synthesis for Higher Order Logic Locking. Lecture Notes in Computer Science, 2022, , 3-24.	1.3	9
143	Detecting Hardware Trojans in PCBs Using Side Channel Loopbacks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 926-937.	3.1	9
144	Improving GPU Robustness by making use of faulty parts. , 2011, , .		8

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145	Secure design-for-debug for Systems-on-Chip. , 2015, , .		8
146	Securing pressure measurements using SensorPUFs. , 2016, , .		8
147	TAINT: Tool for Automated INsertion of Trojans. , 2017, , .		8
148	COPPTCHA: COPPA Tracking by Checking Hardware-Level Activity. IEEE Transactions on Information Forensics and Security, 2020, 15, 3213-3226.	6.9	8
149	Programmable Daisychaining of Microelectrodes to Secure Bioassay IP in MEDA Biochips. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1269-1282.	3.1	8
150	How Secure Are Checkpoint-Based Defenses in Digital Microfluidic Biochips?. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 143-156.	2.7	8
151	Toward Hardware-Based IP Vulnerability Detection and Post-Deployment Patching in Systems-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1158-1171.	2.7	8
152	Causative Cyberattacks on Online Learning-Based Automated Demand Response Systems. IEEE Transactions on Smart Grid, 2021, 12, 3548-3559.	9.0	8
153	Thwarting Bio-IP Theft Through Dummy-Valve-Based Obfuscation. IEEE Transactions on Information Forensics and Security, 2021, 16, 2076-2089.	6.9	8
154	Algorithm level re-computing using implementation diversity: a register transfer level concurrent error detection technique. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 864-875.	3.1	7
155	AES design space exploration new line for scan attack resiliency. , 2014, , .		7
156	NREPO: Normal basis Recomputing with Permuted Operands. , 2014, , .		7
157	Exploiting Small Leakages in Masks to Turn a Second-Order Attack into a First-Order Attack and Improved Rotating Substitution Box Masking with Linear Code Cosets. Scientific World Journal, The, 2015, 2015, 1-10.	2.1	7
158	Secure and Flexible Trace-Based Debugging of Systems-on-Chip. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-25.	2.6	7
159	Shadow attacks on MEDA biochips. , 2018, , .		7
160	High-Level Synthesis of Benevolent Trojans. , 2019, , .		7
161	Security Assessment of Microfluidic Fully-Programmable-Valve-Array Biochips. , 2019, , .		7
162	Stealthy Rootkits in Smart Grid Controllers. , 2019, , .		7

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163	Efficient Hardware Implementation of PQC Primitives and PQC algorithms Using High-Level Synthesis. , 2021, , .		7
164	Attacking a CNN-based Layout Hotspot Detector Using Group Gradient Method. , 2021, , .		7
165	Secure Assay Execution on MEDA Biochips to Thwart Attacks Using Real-Time Sensing. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-25.	2.6	7
166	Molecular Barcoding as a Defense Against Benchtop Biochemical Attacks on DNA Fingerprinting and Information Forensics. IEEE Transactions on Information Forensics and Security, 2020, 15, 3595-3609.	6.9	7
167	Divide-and-concatenate: an architecture level optimization technique for universal hash functions. , 2004, , .		6
168	Deep Packet Field Extraction Engine (DPFEE): A pre-processor for network intrusion detection and denial-of-service detection systems. , 2015, , .		6
169	Controlling your control flow graph. , 2016, , .		6
170	Process-aware side channel monitoring for embedded control system security. , 2017, , .		6
171	On the Difficulty of Inserting Trojans in Reversible Computing Architectures. IEEE Transactions on Emerging Topics in Computing, 2018, , 1-1.	4.6	6
172	Tamper-resistant pin-constrained digital microfluidic biochips. , 2018, , .		6
173	Abetting Planned Obsolescence by Aging 3D Networks-on-Chip. , 2018, , .		6
174	Power, Area, Speed, and Security (PASS) Trade-Offs of NIST PQC Signature Candidates Using a C to ASIC Design Flow. , 2019, , .		6
175	Synthesis of Tamper-Resistant Pin-Constrained Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 171-184.	2.7	6
176	Bio-chemical Assay Locking to Thwart Bio-IP Theft. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-20.	2.6	6
177	Special Session: Machine Learning for Semiconductor Test and Reliability. , 2021, , .		6
178	Design of a high-performance RSVP-TE hardware signaling accelerator. IEEE Journal on Selected Areas in Communications, 2005, 23, 1588-1595.	14.0	5
179	Towards Nanoelectronics Processor Architectures. Journal of Electronic Testing: Theory and Applications (JETTA), 2007, 23, 235-254.	1.2	5
180	Feasibility study of dynamic Trusted Platform Module. , 2010, , .		5

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181	Reusing the IEEE 1500 design for test infrastructure for security monitoring of Systems-on-Chip. , 2014, , .		5
182	Special Issue on Emerging Nanoscale Architectures for Hardware Security, Trust, and Reliability: Part 1. IEEE Transactions on Emerging Topics in Computing, 2014, 2, 2-3.	4.6	5
183	Boolean Circuit Camouflage. , 2017, , .		5
184	Toward Secure Checkpointing for Micro-Electrode-Dot-Array Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4908-4920.	2.7	5
185	Security Against Data-Sniffing and Alteration Attacks in IJTAG. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1301-1314.	2.7	5
186	HOST: HLS Obfuscations against SMT ATtack. , 2021, , .		5
187	A Composable Design Space Exploration Framework to Optimize Behavioral Locking. , 2022, , .		5
188	Synthesis of fault-tolerant and real-time microarchitectures. Journal of Systems and Software, 1994, 25, 73-84.	4.5	4
189	Tamper Proofing by Design Using Generalized Involution-Based Concurrent Error Detection for Involutional Substitution Permutation and Feistel Networks. IEEE Transactions on Computers, 2006, 55, 1230-1239.	3.4	4
190	Parallel memristors: Improving variation tolerance in memristive digital circuits. , 2011, , .		4
191	A Survey of Microarchitecture Support for Embedded Processor Security. , 2012, , .		4
192	Low-Cost Concurrent Error Detection for GCM and CCM. Journal of Electronic Testing: Theory and Applications (JETTA), 2014, 30, 725.	1.2	4
193	Trustworthy Hardware [Scanning the Issue]. Proceedings of the IEEE, 2014, 102, 1123-1125.	21.3	4
194	IC/IP piracy assessment of reversible logic. , 2018, , .		4
195	Locking the Design of Building Blocks for Quantum Circuits. Transactions on Embedded Computing Systems, 2019, 18, 1-15.	2.9	4
196	Identification of Synthesis Approaches for IP/IC Piracy of Reversible Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-17.	2.3	4
197	Programmable Daisychaining of Microelectrodes for IP Protection in MEDA Biochips. , 2019, , .		4
198	Anomaly Detection in Embedded Systems Using Power and Memory Side Channels. , 2020, , .		4

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199	Detecting Kernel Control-Flow Modifying Rootkits. Advances in Information Security, 2014, , 177-187.	1.2	4
200	Protection against Counterfeiting Attacks in 3D Printing by Streaming Signature-embedded Manufacturing Process Instructions. , 2021, , .		4
201	Trojan Detection in Embedded Systems With FinFET Technology. IEEE Transactions on Computers, 2022, 71, 3061-3071.	3.4	4
202	Learning Malicious Circuits in FPGA Bitstreams. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 726-739.	2.7	4
203	Standard seven segmented display for Burmese numerals. IEEE Transactions on Consumer Electronics, 1990, 36, 959-961.	3.6	3
204	?â„°â„±ect ?olerant layout synthesis. International Journal of Electronics, 1994, 76, 1121-1133.	1.4	3
205	Fault-tolerant vlsi systems. IEEE Transactions on Reliability, 1999, 48, 106-107.	4.6	3
206	Selectively breaking data dependences to improve the utilization of idle cycles in algorithm level re-computing data paths. IEEE Transactions on Reliability, 2003, 52, 501-511.	4.6	3
207	Concurrent error detection of fault-based side-channel cryptanalysis of 128-bit RC6 block cipher. Microelectronics Journal, 2003, 34, 31-39.	2.0	3
208	Design automation for hybrid CMOS-nonoelectronics crossbars. , 2007, , .		3
209	Guest Editorial - Integrated Circuit and System Security. IEEE Transactions on Information Forensics and Security, 2012, 7, 1-2.	6.9	3
210	Guest Editorial Special Section on Hardware Security and Trust. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 873-874.	2.7	3
211	Reliable Integrity Checking in Multicore Processors. Transactions on Architecture and Code Optimization, 2015, 12, 1-23.	2.0	3
212	Simulation and analysis of negative-bias temperature instability aging on power analysis attacks. , 2015, , .		3
213	Identifying Reversible Circuit Synthesis Approaches to Enable IP Piracy Attacks. , 2017, , .		3
214	Hardware Trojan detection using path delay order encoding with process variation tolerance. , 2018, , .		3
215	Reversible Circuits: IC/IP Piracy Attacks and Countermeasures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2523-2535.	3.1	3
216	Security Assessment of Microfluidic Immunoassays. , 2019, , .		3

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217	Split Manufacturing-Based Register Transfer-Level Obfuscation. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-22.	2.3	3
218	Analysis and Design of Tamper-Mitigating Microfluidic Routing Fabrics. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1003-1016.	2.7	3
219	Uncertainty quantification in dimensions dataset of additive manufactured NIST standard test artifact. Data in Brief, 2021, 38, 107286.	1.0	3
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