

Seonghwan Cho

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 18-30.	5.4	224
2	A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier. IEEE Journal of Solid-State Circuits, 2013, 48, 1009-1017.	5.4	138
3	A 9 bit, 1.12 ps Resolution 2.5 b/Stage Pipelined Time-to-Digital Converter in 65 nm CMOS Using Time-Register. IEEE Journal of Solid-State Circuits, 2014, 49, 1007-1016.	5.4	125
4	A 14.2 mW 2.55-to-3 GHz Cascaded PLL With Reference Injection and 800 MHz Delta-Sigma Modulator in 0.13 μm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 2989-2998.	5.4	99
5	A 1.4- μW 24.9-ppm/ $^{\circ}\text{C}$ Current Reference With Process-Insensitive Temperature Compensation in 0.18- μm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 2527-2533.	5.4	65
6	A 2.4 GHz Fractional-N Frequency Synthesizer With High-OSR $\Sigma\Delta$ Modulator and Nested PLL. IEEE Journal of Solid-State Circuits, 2012, 47, 2433-2443.	5.4	56
7	Integrated All Electrical Pulse Wave Velocity and Respiration Sensors Using Bio-Impedance. IEEE Journal of Solid-State Circuits, 2015, 50, 776-785.	5.4	56
8	A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 3571-3581.	5.4	55
9	A 0.22 ps rms Integrated Noise 15 MHz Bandwidth Fourth-Order $\Sigma\Delta$ Time-to-Digital Converter Using Time-Domain Error-Feedback Filter. IEEE Journal of Solid-State Circuits, 2015, 50, 1251-1262.	5.4	49
10	A 6.5-GHz energy-efficient BFSK modulator for wireless sensor applications. IEEE Journal of Solid-State Circuits, 2004, 39, 731-739.	5.4	42
11	Design Techniques for a Low-Voltage VCO With Wide Tuning Range and Low Sensitivity to Environmental Variations. IEEE Transactions on Microwave Theory and Techniques, 2009, 57, 767-774.	4.6	41
12	An Ultra-High Input Impedance Analog Front End Using Self-Calibrated Positive Feedback. IEEE Journal of Solid-State Circuits, 2018, 53, 2252-2262.	5.4	40
13	A 2.92- μW Capacitance-to-Digital Converter With Differential Bondwire Accelerometer, On-Chip Air Pressure, and Humidity Sensor in 0.18- μm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 2845-2856.	5.4	38
14	A $148\text{fs}_{\text{rms}}$ Integrated Noise 4 MHz Bandwidth Second-Order $\Sigma\Delta$ Time-to-Digital Converter With Gated Switched-Ring Oscillator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2281-2289.	5.4	34
15	A 2.4-GHz 1.5-mW Digital Multiplying Delay-Locked Loop Using Pulsewidth Comparator and Double Injection Technique. IEEE Journal of Solid-State Circuits, 2017, 52, 2934-2946.	5.4	32
16	A 7b, 3.75ps resolution two-step time-to-digital converter in 65nm CMOS using pulse-train time amplifier. , 2012, , .		29
17	A Time-Domain High-Order MASH $\Sigma\Delta$ ADC Using Voltage-Controlled Gated-Ring Oscillator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 856-866.	5.4	28
18	A Low-Power Photoplethysmogram-Based Heart Rate Sensor Using Heartbeat Locked Loop. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 1220-1229.	4.0	27

#	ARTICLE	IF	CITATIONS
19	A 24.8- μ W Biopotential Amplifier Tolerant to 15-V _{PP} Common-Mode Interference for Two-Electrode ECG Recording in 180-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 591-600.	5.4	24
20	A 2.5-Gb/s On-Chip Interconnect Transceiver With Crosstalk and ISI Equalizer in 130 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 124-136.	5.4	22
21	A Highly-Digital VCO-Based Analog-to-Digital Converter Using Phase Interpolator and Digital Calibration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1368-1372.	3.1	21
22	A 0.8V, 37nW, 42ppm/ $^{\circ}$ C sub-bandgap voltage reference with PSRR of \sim 81dB and line sensitivity of 51ppm/V in 0.18 μ m CMOS. , 2017, , .		21
23	A Hybrid-Domain Two-Step Time-to-Digital Converter Using a Switch-Based Time-to-Voltage Converter and SAR ADC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 631-635.	3.0	20
24	A Single BJT Bandgap Reference With Frequency Compensation Exploiting Mirror Pole. IEEE Journal of Solid-State Circuits, 2021, 56, 2902-2912.	5.4	17
25	A 1.8 V 900 μ W 4.5 GHz VCO and Prescaler in 0.18 μ m CMOS Using Charge-Recycling Technique. IEEE Microwave and Wireless Components Letters, 2009, 19, 104-106.	3.2	14
26	A Second-Order $\Delta\Sigma$ Time-to-Digital Converter Using Highly Digital Time-Domain Arithmetic Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1643-1647.	3.0	13
27	A 470- μ W 5-GHz Digitally Controlled Injection-Locked Multi-Modulus Frequency Divider With an In-Phase Dual-Input Injection Scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 61-70.	3.1	12
28	A supply noise insensitive PLL with a rail-to-rail swing ring oscillator and a wideband noise suppression loop. , 2017, , .		12
29	A 0.0082-mm 2 , 192-nW Single BJT Branch Bandgap Reference in 0.18- μ m CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 426-429.	2.0	12
30	An Optimum Current Mirror Ratio for Low Phase Noise LC-VCO. IEEE Microwave and Wireless Components Letters, 2008, 18, 809-811.	3.2	11
31	A Low-Noise and Low-Power Frequency Synthesizer Using Offset Phase-Locked Loop in 0.13- μ m CMOS. IEEE Microwave and Wireless Components Letters, 2010, 20, 52-54.	3.2	11
32	A 1-GS/s 9-bit Zero-Crossing-Based Pipeline ADC Using a Resistor as a Current Source. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2570-2579.	3.1	10
33	A Sleep Apnea Monitoring IC for Respiration, Heart-Rate, SpO ₂ and Pulse-Transit Time Measurement Using Thermistor, PPG and Body-Channel Communication. IEEE Sensors Journal, 2020, 20, 1997-2007.	4.7	10
34	A 10-bit 300MSample/s pipelined ADC using time-interleaved SAR ADC for front-end stages. , 2010, , .		8
35	A ring oscillator-based temperature sensor for u-healthcare in 0.13- μ m cmos. , 2009, , .		7
36	CMRR enhancement technique for IA using three IAs for bio-medical sensor applications. , 2010, , .		6

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37	Time-interleaved single-slope ADC using counter-based time-to-digital converter. , 2011, , .		6
38	A 2.3-mW 0.01-mm \times 1.25-GHz Quadrature Signal Corrector With 1.1-ps Error for Mobile DRAM Interface in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 397-401.	3.0	6
39	Close-in phase-noise enhanced voltage-controlled oscillator employing parasitic V-NPN transistor in CMOS process. IEEE Transactions on Microwave Theory and Techniques, 2006, 54, 1363-1369.	4.6	5
40	A Relative Permittivity-Based Air Pressure Sensor Using Standard CMOS Process. IEEE Sensors Journal, 2017, 17, 3892-3899.	4.7	5
41	An On-Chip Thermal Monitoring System With a Temperature Sensing Area of $52 \mu\text{m}^2$ in 180-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1638-1642.	3.0	5
42	An ultra low power UHF RFID tag front-end for EPCglobal Gen2 with novel clock-free decoder. , 2008, , .		4
43	A 1.8 to 2.4-GHz 20mW digital-intensive RF sampling receiver with a noise-canceling bandpass low-noise amplifier in 90nm CMOS. , 2010, , .		4
44	A Hybrid PLL Using Low-Power GRO-TDC for Reduced In-Band Phase Noise. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 232-236.	3.0	4
45	22.4 A 27.8 μ W Biopotential Amplifier Tolerant to 30V pp Common-Mode Interference for Two-Electrode ECG Recording in 0.18 μ m CMOS. , 2019, , .		4
46	A 43.3 μ W Biopotential Amplifier With Tolerance to Common-Mode Interference of 18 V pp and T-CMRR of 105 dB in 180-nm CMOS. IEEE Journal of Solid-State Circuits, 2023, 58, 508-519.	5.4	4
47	A Quadrature Modulation Transmitter Using Two Frequency Synthesizers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 907-911.	3.0	3
48	A Digital-Intensive Multimode Multiband Receiver Using a Sinc 2 Filter-Embedded VCO-Based ADC. IEEE Transactions on Microwave Theory and Techniques, 2012, 60, 3254-3262.	4.6	3
49	A 2.69 μ W Dual Quantization-Based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18 μ m CMOS. , 2018, , .		3
50	A 3.2-GHz Supply Noise-Insensitive PLL Using a Gate-Voltage-Boosted Source-Follower Regulator and Residual Noise Cancellation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2170-2174.	3.1	3
51	A Low Power Transmitter for Phase-Shift Keying Modulation Schemes. , 2006, , .		2
52	A 2.4-GHz reference doubled fractional-N PLL with dual phase detector in 0.13 μ m CMOS. , 2010, , .		2
53	A PVT tolerant BPF using turn-off MOSFET for bio applications in 0.13 μ m CMOS. , 2010, , .		2
54	A High-Frequency Compensated Crosstalk and ISI Equalizer for Multi-Channel On-Chip Interconnect in 130-nm CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 314-321.	3.6	2

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55	A Capacitance-to-Digital Converter with Differential Bondwire Accelerometer, On-chip Air Pressure and Humidity Sensor in 0.18 μm CMOS. , 2020, , .		2
56	An Energy-Efficient Voltage Step-up System for 3D NAND Flash using Charge-Compensating Regulator. , 2021, , .		2
57	A 900 MHz 2.2 mW spread spectrum clock generator based on direct frequency synthesis and harmonic injection locking. , 2009, , .		1
58	A time-based successive approximation register analog-to-digital converter using a pulse width modulation technique with a single capacitor. , 2009, , .		1
59	28.6 A 22.6 μW Biopotential Amplifier with Adaptive Common-Mode Interference Cancellation Achieving Total-CMRR of 104dB and CMI Tolerance of 15V _{pp} in 0.18 μm CMOS. , 2021, , .		1
60	A 43 nW, 32 kHz, $\hat{\Delta}\pm 4.2$ ppm Piecewise Linear Temperature-Compensated Crystal Oscillator With $\hat{\Gamma}\hat{\Gamma}\hat{\Gamma}$ -Modulated Load Capacitance. IEEE Journal of Solid-State Circuits, 2022, 57, 1175-1186.	5.4	1
61	A time-domain flash ADC immune to voltage controlled delay line non-linearity. , 2011, , .		0
62	All electrical and real-time ECG, respiration, airflow, and skin conductance monitoring system. , 2015, , .		0
63	A supply noise insensitive PLL with a rail-to-rail swing ring oscillator and a wideband noise suppression loop. , 2018, , .		0
64	An On-Off Keying LC Oscillator-Based Acoustic Transmitter with Fast Turn-On and Turn-Off Time. , 2019, , .		0
65	A Low-Power Piezoelectric Speaker Driver Using LC Oscillator for Acoustic Communication. , 2019, , .		0
66	A Low-Jitter Area-Efficient LC-VCO Based Clock Generator in 0.13- μm CMOS. IEICE Transactions on Electronics, 2009, E92-C, 589-591.	0.6	0
67	An Ultra Low Power and Variation Tolerant GEN2 RFID Tag Front-End with Novel Clock-Free Decoder. IEICE Transactions on Electronics, 2010, E93-C, 785-795.	0.6	0