Shuvra S Bhattacharyya

List of Publications by Year
in descending order

252 papers	2,717 citations	430754 18 h-index	330025 37 g-index
265 all docs	265 docs citations	265 times ranked	1145 citing authors

#	Article	IF	Citations
1	Hyperspectral Image Classification With Attention-Aided CNNs. IEEE Transactions on Geoscience and Remote Sensing, 2021, 59, 2281-2293.	2.7	200
2	Parameterized dataflow modeling for DSP systems. IEEE Transactions on Signal Processing, 2001, 49, 2408-2421.	3.2	197
3	Synthesis of Embedded Software from Synchronous Dataflow Specifications. Journal of Signal Processing Systems, 1999, 21, 151-166.	1.0	150
4	Overview of the MPEG Reconfigurable Video Coding Framework. Journal of Signal Processing Systems, 2011, 63, 251-263.	1.4	81
5	Gabriel: a design environment for DSP. IEEE Transactions on Acoustics, Speech, and Signal Processing, 1989, 37, 1751-1762.	2.0	78
6	Functional DIF for Rapid Prototyping. , 2008, , .		72
7	Systematic Integration of Parameterized Local Search Into Evolutionary Algorithms. IEEE Transactions on Evolutionary Computation, 2004, 8, 137-155.	7.5	63
8	Software synthesis from the dataflow interchange format. , 2005, , .		57
9	OpenDF. Computer Architecture News, 2008, 36, 29-35.	2.5	56
10	PiMM: Parameterized and Interfaced dataflow Meta-Model for MPSoCs runtime reconfiguration. , 2013, , .		54
11	Joint Minimization of Code and Data for Synchronous Dataflow Programs. Formal Methods in System Design, 1997, 11, 41-70.	0.9	52
12	Intermediate Representations for Design Automation of Multiprocessor DSP Systems. Design Automation for Embedded Systems, 2002, 7, 307-323.	0.7	39
13	Title is missing!. Design Automation for Embedded Systems, 1997, 2, 33-60.	0.7	38
14	Efficient techniques for clustering and scheduling onto embedded multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2006, 17, 667-680.	4.0	37
15	A generalized static data flow clustering algorithm for mpsoc scheduling of multimedia applications. , 2008, , .		35
16	Scheduling synchronous dataflow graphs for efficient looping. Journal of Signal Processing Systems, 1993, 6, 271-288.	1.0	34
17	Buffer mergingâ€"a powerful technique for reducing memory requirements of synchronous dataflow specifications. ACM Transactions on Design Automation of Electronic Systems, 2004, 9, 212-237.	1.9	34
18	Parameterized Looped Schedules for Compact Representation of Execution Sequences in DSP Hardware and Software Implementation. IEEE Transactions on Signal Processing, 2007, 55, 3126-3138.	3.2	28

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19	Memory management for dataflow programming of multirate signal processing algorithms. IEEE Transactions on Signal Processing, 1994, 42, 1190-1201.	3.2	27
20	A generalized scheduling approach for dynamic dataflow applications. , 2009, , .		24
21	Evolutionary algorithms for the synthesis of embedded software. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 452-455.	2.1	22
22	Interface-based hierarchy for synchronous data-flow graphs. , 2009, , .		22
23	An Energy-Driven Design Methodology for Distributing DSP Applications across Wireless Sensor Networks. , 2007, , .		21
24	Exploiting Statically Schedulable Regions in Dataflow Programs. Journal of Signal Processing Systems, 2011, 63, 129-142.	1.4	21
25	Heterogeneous Design in Functional DIF. Lecture Notes in Computer Science, 2008, , 157-166.	1.0	21
26	Exploiting statically schedulable regions in dataflow programs. , 2009, , .		20
27	Exploring the Concurrency of an MPEG RVC Decoder Based on Dataflow Program Analysis. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1646-1657.	5.6	20
28	Dynamic Dataflow Graphs. , 2013, , 905-944.		20
29	Joint application mapping/interconnect synthesis techniques for embedded chip-scale multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2005, 16, 99-112.	4.0	19
30	Dynamic, data-driven processing of multispectral video streams. IEEE Aerospace and Electronic Systems Magazine, 2017, 32, 50-57.	2.3	18
31	An integrated hardware/software design methodology for signal processing systems. Journal of Systems Architecture, 2019, 93, 1-19.	2.5	18
32	Optimizing synchronization in multiprocessor DSP systems. IEEE Transactions on Signal Processing, 1997, 45, 1605-1618.	3.2	16
33	Energy-Aware Data Compression for Wireless Sensor Networks. , 2007, , .		16
34	Looped schedules for dataflow descriptions of multirate signal processing algorithms. Formal Methods in System Design, 1994, 5, 183-205.	0.9	15
35	Design and implementation of embedded computer vision systems based on particle filters. Computer Vision and Image Understanding, 2010, 114, 1203-1214.	3.0	15
36	Mobile transmitter digital predistortion: Feasibility analysis, algorithms and design exploration. , 2013, , .		14

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37	Reproducible Evaluation of System Efficiency With a Model of Architecture: From Theory to Practice. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2050-2063.	1.9	14
38	PRUNE: Dynamic and Decidable Dataflow for Signal Processing on Heterogeneous Platforms. IEEE Transactions on Signal Processing, 2018, 66, 654-665.	3.2	14
39	Elastic Neural Networks: A Scalable Framework for Embedded Computer Vision. , 2018, , .		14
40	DIF: An Interchange Format for Dataflow-Based Design Tools. Lecture Notes in Computer Science, 2004, , 423-432.	1.0	14
41	Compact Procedural Implementation in DSP Software Synthesis Through Recursive Graph Decomposition. Lecture Notes in Computer Science, 2004, , 47-61.	1.0	14
42	Modeling of Block-Based DSP Systems. Journal of Signal Processing Systems, 2005, 40, 289-299.	1.0	13
43	Efficient simulation of critical synchronous dataflow graphs. , 2006, , .		13
44	Energy-driven distribution of signal processing applications across wireless sensor networks. ACM Transactions on Sensor Networks, 2010, 6, 1-32.	2.3	13
45	FPGA-based design and implementation of the 3GPP-LTE physical layer using parameterized synchronous dataflow techniques. , 2010, , .		13
46	Dynamic Dataflow Graphs. , 2019, , 1173-1210.		13
47	Applying graphics processor acceleration in a software defined radio prototyping environment. , 2011, , .		12
48	Parameterized Sets of Dataflow Modes And Their Application to Implementation of Cognitive Radio Systems. Journal of Signal Processing Systems, 2015, 80, 3-18.	1.4	12
49	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems. , 2017, , 1185-1219.		12
50	Multidimensional Exploration of Software Implementations for DSP Algorithms. Journal of Signal Processing Systems, 2000, 24, 83-98.	1.0	11
51	Adaptive negative cycle detection in dynamic graphs. , 2001, , .		11
52	Efficient simulation of critical synchronous dataflow graphs. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 1-28.	1.9	11
53	Dataflow-Based Mapping of Computer Vision Algorithms onto FPGAs. Eurasip Journal on Embedded Systems, 2007, 2007, 1-12.	1.2	11
54	Model-based mapping of reconfigurable image registration on FPGA platforms. Journal of Real-Time Image Processing, 2008, 3, 149-162.	2.2	11

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55	Signal processing on platforms with multiple cores: Part 1 - Overview and methodologies [From the Guest Editors. IEEE Signal Processing Magazine, 2009, 26, 24-25.	4.6	11
56	A Model-Based Schedule Representation for Heterogeneous Mapping of Dataflow Graphs. , 2011, , .		11
57	Pipelined FFT for wireless communications supporting 128–2048 / 1536 -point transforms. , 2013, , .		11
58	A novel view synthesis approach based on view space covering for gait recognition. Neurocomputing, 2021, 453, 13-25.	3.5	11
59	Shared memory implementations of synchronous dataflow specifications. , 2000, , .		10
60	Memory-constrained Block Processing for DSP Software Optimization. Journal of Signal Processing Systems, 2008, 50, 163-177.	1.4	10
61	Mode grouping for more effective generalized scheduling of dynamic dataflow applications. , 2009, , .		10
62	Analysis of SystemC actor networks for efficient synthesis. Transactions on Embedded Computing Systems, 2010, 10, 1-34.	2.1	10
63	Integration of Dataflow-Based Heterogeneous Multiprocessor Scheduling Techniques in GNU Radio. Journal of Signal Processing Systems, 2013, 70, 177-191.	1.4	10
64	Low-Complexity Digital Predistortion for Reducing Power Amplifier Spurious Emissions in Spectrally-Agile Flexible Radio. , 2014, , .		10
65	Multi-Scale Gradient Image Super-Resolution for Preserving SIFT Key Points in Low-Resolution Images. Signal Processing: Image Communication, 2019, 78, 236-245.	1.8	10
66	Reconfigurable image registration on FPGA platforms. , 2006, , .		9
67	Towards a Heterogeneous Medical Image Registration Acceleration Platform. , 2007, , .		9
68	Multithreaded simulation for synchronous dataflow graphs. , 2008, , .		9
69	Resource-efficient acceleration of 2-dimensional Fast Fourier Transform computations on FPGAs. , 2009, , .		9
70	Mapping Parameterized Cyclo-static Dataflow Graphs onto Configurable Hardware. Journal of Signal Processing Systems, 2012, 66, 285-301.	1.4	9
71	Model Based Design Environment for Data-driven Embedded Signal Processing Systems1. Procedia Computer Science, 2014, 29, 1193-1202.	1.2	9
72	Resource-constrained implementation and optimization of a deep neural network for vehicle classification. , 2016, , .		9

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73	Weakly supervised segmentation for realâ€time surgical tool tracking. Healthcare Technology Letters, 2019, 6, 231-236.	1.9	9
74	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems. , 2016, , 1-35.		9
75	Dataflow Transformations in High-level DSP System Design. , 2006, , .		8
76	Affine Nested Loop Programs and their Binary Parameterized Dataflow Graph Counterparts. , 2006, , .		8
77	A taxonomy for medical image registration acceleration techniques. , 2007, , .		8
78	Low-Overhead Run-Time Scheduling for Fine-Grained Acceleration of Signal Processing Systems. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	8
79	Parameterized design framework for hardware implementation of particle filters. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	8
80	Design and Synthesis for Multimedia Systems Using the Targeted Dataflow Interchange Format. IEEE Transactions on Multimedia, 2012, 14, 630-640.	5.2	8
81	Efficient architecture mapping of FFT/IFFT for cognitive radio networks. , 2014, , .		8
82	Compact modeling and management of reconfiguration in digital channelizer implementation. , 2016, , .		8
83	A Hybrid Task Graph Scheduler for High Performance Image Processing Workflows. Journal of Signal Processing Systems, 2017, 89, 457-467.	1.4	8
84	Efficient Solving of Markov Decision Processes on GPUs Using Parallelized Sparse Matrices. , 2018, , .		8
85	Gradient Image Super-resolution for Low-resolution Image Recognition. , 2019, , .		8
86	Memory-Constrained Vectorization and Scheduling of Dataflow Graphs for Hybrid CPU-GPU Platforms. Transactions on Embedded Computing Systems, 2018, 17, 1-25.	2.1	8
87	Contention-conscious transaction ordering in multiprocessor DSP systems. IEEE Transactions on Signal Processing, 2006, 54, 556-569.	3.2	7
88	Systematic generation of FPGA-based FFT implementations. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	7
89	A novel framework for design and implementation of adaptive stream mining systems. , 2013, , .		7
90	Low power implementation of digital predistortion filter on a heterogeneous application specific multiprocessor. , 2014, , .		7

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91	Implementation of a low-complexity low-latency arbitrary resampler on GPUs. , 2014, , .		7
92	A Design Framework for Mapping Vectorized Synchronous Dataflow Graphs onto CPU-GPU Platforms. , 2016, , .		7
93	Implementation, Scheduling, and Adaptation of Partial Expansion Graphs on Multicore Platforms. Journal of Signal Processing Systems, 2017, 87, 107-125.	1.4	7
94	An accumulative fusion architecture for discriminating people and vehicles using acoustic and seismic signals. , 2017, , .		7
95	Online learning in neural decoding using incremental linear discriminant analysis. , 2017, , .		7
96	Model-based cosimulation for industrial wireless networks. , 2018, , .		7
97	Model-Based Mapping of Image Registration Applications onto Configurable Hardware. , 2006, , .		6
98	Multiobjective Optimization of FPGA-Based Medical Image Registration. , 2008, , .		6
99	Towards systematic exploration of tradeoffs for medical image registration on heterogeneous platforms. , 2008, , .		6
100	Design and optimization of a distributed, embedded speech recognition system. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	6
101	A Low-overhead Scheduling Methodology for Fine-grained Acceleration of Signal Processing Systems. Journal of Signal Processing Systems, 2010, 60, 333-343.	1.4	6
102	Scalable representation of dataflow graph structures using topological patterns. , 2010, , .		6
103	Topological Patterns for Scalable Representation and Analysis of Dataflow Graphs. Journal of Signal Processing Systems, 2011, 65, 229-244.	1.4	6
104	Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications. , 2012, , .		6
105	Implementation of a high-throughput low-latency polyphase channelizer on GPUs. Eurasip Journal on Advances in Signal Processing, 2014, 2014, .	1.0	6
106	A hybrid task graph scheduler for high performance image processing workflows. , 2015, , .		6
107	A Wideband Front-End Receiver Implementation on GPUs. IEEE Transactions on Signal Processing, 2016, 64, 2602-2612.	3.2	6
108	Real-Time Neuron Detection and Neural Signal Extraction Platform for Miniature Calcium Imaging. Frontiers in Computational Neuroscience, 2020, 14, 43.	1.2	6

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109	Prinet: A Prior Driven Spectral Super-Resolution Network. , 2020, , .		6
110	DSP address optimization using evolutionary algorithms. , 2005, , .		5
111	A Communication Interface for Multiprocessor Signal Processing Systems. , 2006, , .		5
112	Analysis of Dataflow Programs with Interval-limited Data-rates. Journal of Signal Processing Systems, 2006, 43, 247-258.	1.0	5
113	Model-based design and implementation of an adaptive digital predistortion filter. , 2015, , .		5
114	Introduction to Hardware/Software Codesign. , 2017, , 3-26.		5
115	Hardware design methodology using lightweight dataflow and its integration with low power techniques. Journal of Systems Architecture, 2017, 78, 15-29.	2.5	5
116	Real-Time Calcium Imaging Based Neural Decoding with a Support Vector Machine. , 2019, , .		5
117	Energy-Driven Partitioning of Signal Processing Algorithms in Sensor Networks. Lecture Notes in Computer Science, 2006, , 142-154.	1.0	5
118	Segmentation of surgical instruments in laparoscopic videos: training dataset generation and deep-learning-based framework. , 2019, , .		5
119	The hierarchical timing pair model for multirate DSP applications. IEEE Transactions on Signal Processing, 2004, 52, 1209-1217.	3.2	4
120	Memory-constrained Block Processing Optimization for Synthesis of DSP Software. , 2006, , .		4
121	The pipeline decomposition tree:. , 2006, , .		4
122	Beyond single-appearance schedules. Transactions on Embedded Computing Systems, 2007, 6, 14.	2.1	4
123	Compact, Low Power Wireless Sensor Network System for Line Crossing Recognition. , 2007, , .		4
124	Advances in hardware design and implementation of signal processing systems [DSP Forum]. IEEE Signal Processing Magazine, 2008, 25, 175-180.	4.6	4
125	Sensor Support Systems for Asymmetric Threat Countermeasures. IEEE Sensors Journal, 2008, 8, 682-692.	2.4	4
126	Multiobjective Optimization for Reconfigurable Implementation of Medical Image Registration. International Journal of Reconfigurable Computing, 2008, 2008, 1-17.	0.2	4

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127	Dataflow-based implementation of model predictive control. , 2009, , .		4
128	High-Performance Buffer Mapping to Exploit DRAM Concurrency in Multiprocessor DSP Systems. , 2009, , .		4
129	An architectural level design methodology for smart camera applications. International Journal of Embedded Systems, 2009, 4, 83.	0.2	4
130	Efficient static buffering to guarantee throughput-optimal FPGA implementation of synchronous dataflow graphs. , 2010, , .		4
131	Utilizing Hierarchical Multiprocessing for Medical Image Registration. IEEE Signal Processing Magazine, 2010, 27, 61-68.	4.6	4
132	Signal Processing on Platforms with Multiple Cores: Part 2-Applications and Design [From the Guest Editors. IEEE Signal Processing Magazine, 2010, 27, 20-21.	4.6	4
133	Vectorization and mapping of software defined radio applications on heterogeneous multi-processor platforms. , 2011, , .		4
134	Just-in-time scheduling techniques for multicore signal processing systems. , 2014, , .		4
135	Multiobjective Design Optimization in the Lightweight Dataflow for DDDAS Environment (LiD4E) 1. Procedia Computer Science, 2015, 51, 2563-2572.	1.2	4
136	Constant-rate clock recovery and jitter measurement on deep memory waveforms using dataflow. , 2015, , .		4
137	Models of Architecture: Reproducible Efficiency Evaluation for Signal Processing Systems. , 2016, , .		4
138	An optimized embedded target detection system using acoustic and seismic sensors. , 2017, , .		4
139	Model-based dynamic scheduling for multicore implementation of image processing systems. , 2017, , .		4
140	Elastic Neural Networks for Classification. , 2019, , .		4
141	Design Space Exploration for Wireless-Integrated Factory Automation Systems. , 2019, , .		4
142	Research Challenges for Heterogeneous Cyberphysical System Design. Computer, 2020, 53, 71-75.	1.2	4
143	Heterogeneous Design in Functional DIF. Lecture Notes in Computer Science, 2011, , 391-408.	1.0	4
144	Scheduling of Synchronous Dataflow Graphs with Partially Periodic Real-Time Constraints. , 2020, , .		4

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145	Neural decoding on imbalanced calcium imaging data with a network of support vector machines. Advanced Robotics, 2021, 35, 459-470.	1.1	4
146	Design Methodology for Embedded Computer Vision Systems. , 2009, , 27-47.		4
147	The CBP Parameter: A Module Characterization Approach for DSP Software Optimization. Journal of Signal Processing Systems, 2004, 38, 131-146.	1.0	3
148	A Rapid Prototyping Methodology for Application-Specific Sensor Networks. , 2006, , .		3
149	Methods for efficient implementation of Model Predictive Control on multiprocessor systems. , 2010, , .		3
150	Loop transformations for interface-based hierarchies IN SDF graphs. , 2010, , .		3
151	Design methods for Wireless Sensor Network Building Energy Monitoring Systems. , 2011, , .		3
152	Multidimensional Dataflow Graph Modeling and Mapping for Efficient GPU Implementation. , 2012, , .		3
153	Configurable, resource-optimized FFT architecture for OFDM communication. , 2013, , .		3
154	Reconfigurable Digital Channelizer Design Using Factored Markov Decision Processes. Journal of Signal Processing Systems, 2018, 90, 1329-1343.	1.4	3
155	Incremental Deep Neural Network Pruning Based on Hessian Approximation. , 2019, , .		3
156	CGMBE: a model-based tool for the design and implementation of real-time image processing applications on CPUâ€“GPU platforms. Journal of Real-Time Image Processing, 2021, 18, 561-583.	2.2	3
157	Learning Compact DNN Models for Behavior Prediction from Neural Activity of Calcium Imaging. Journal of Signal Processing Systems, 2022, 94, 455-472.	1.4	3
158	Dynamic and Multidimensional Dataflow Graphs. , 2010, , 899-930.		3
159	Logic Foundry: Rapid Prototyping for FPGA-Based DSP Systems. Eurasip Journal on Advances in Signal Processing, 2003, 2003, 1.	1.0	2
160	Configuration and Representation of Large-Scale Dataflow Graphs using the Dataflow Interchange Format. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2006, , .	0.0	2
161	An integrated ASIP design flow for digital signal processing applications. , 2008, , .		2
162	Improving the performance of active set based Model Predictive Controls by dataflow methods. , 2009, , .		2

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163	Simulating dynamic communication systems using the core functional dataflow model. , 2010, , .		2
164	Rapid prototyping for digital signal processing systems using Parameterized Synchronous Dataflow graphs. , 2010, , .		2
165	Multithreaded Simulation for Synchronous Dataflow Graphs. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-23.	1.9	2
166	Parameterized scheduling for signal processing systems using topological patterns. , 2012, , .		2
167	A Design Methodology for Distributed Adaptive Stream Mining Systems. Procedia Computer Science, 2013, 18, 2482-2491.	1.2	2
168	Scheduling of parallelized synchronous dataflow actors. , 2013, , .		2
169	High-performance and low-energy buffer mapping method for multiprocessor DSP systems. Transactions on Embedded Computing Systems, 2013, 12, 1-23.	2.1	2
170	Instrumentation-driven framework for validation of dataflow applications. , 2014, , .		2
171	Scheduling of Parallelized Synchronous Dataflow Actors for Multicore Signal Processing. Journal of Signal Processing Systems, 2016, 83, 309-328.	1.4	2
172	Implementation of a Multirate Resampler for Multi-carrier Systems on GPUs. Journal of Signal Processing Systems, 2017, 89, 445-455.	1.4	2
173	Generalized Graph Connections for Dataflow Modeling of DSP Applications. , 2018, , .		2
174	A Joint Target Localization and Classification Framework for Sensor Networks. , 2018, , .		2
175	Multi-Frame Super Resolution with Deep Residual Learning on Flow Registered Non-Integer Pixel Images. , 2019, , .		2
176	A Framework for Design and Implementation of Adaptive Digital Predistortion Systems. , 2019, , .		2
177	Hyperspectral Video Processing on Resource-Constrained Platforms. , 2019, , .		2
178	MADS: A Framework for Design and Implementation of Adaptive Digital Predistortion Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 712-722.	2.7	2
179	Integrating Field Measurements into a Model-Based Simulator for Industrial Communication Networks. , 2020, , .		2
180	PathTracing: Raising the Level of Understanding of Processing Latency in Heterogeneous MPSoCs. , 2021, , .		2

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181	Instrumentation-Driven Model Detection and Actor Partitioning for Dataflow Graphs. International Journal of Embedded and Real-Time Communication Systems, 2013, 4, 1-21.	0.3	2
182	Optimization of Signal Processing Software for Control System Implementation. , 2006, , .		2
183	Data-Driven Stream Mining Systems for Computer Vision. Advances in Computer Vision and Pattern Recognition, 2014, , 249-264.	0.9	2
184	Evolutionary Multiobjective Optimization for Adaptive Dataflow-based Digital Predistortion Architectures. EAI Endorsed Transactions on Cognitive Communications, 2017, 3, 152187.	0.2	2
185	Dynamic Data Driven Application Systems (DDDAS) for Multimedia Content Analysis. , 2018, , 631-651.		2
186	Design of a Dynamic Data-Driven System for Multispectral Video Processing. , 2018, , 529-545.		2
187	Runtime Adaptation in Wireless Sensor Nodes Using Structured Learning. ACM Transactions on Cyber-Physical Systems, 2020, 4, 1-28.	1.9	2
188	Register File Partitioning with Constraint Programming. , 2006, , .		1
189	Design Techniques for Streamlined Integration and Fault Tolerance in a Distributed Sensor System for Line-crossing Recognition. , 2007, , .		1
190	Synthesis of DSP Architectures Using Libraries of Coarse-Grain Configurations. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	1
191	An Optimized Message Passing Framework for Parallel Implementation of Signal Processing Applications. , 2008, , .		1
192	Trade-offs in mapping high-level dataflow graphs onto ASIPs. , 2008, , .		1
193	Energy efficient implementation of G.729 for wireless VoIP application. , 2008, , .		1
194	Guest Editorial: Special Issue on Multi-Core Enabled Multimedia Applications & Architectures. Journal of Signal Processing Systems, 2009, 57, 121-122.	1.4	1
195	Integration of Dataflow optimization techniques into a software radio design framework. , 2009, , .		1
196	Design and implementation of real-time signal processing applications on heterogeneous multiprocessor arrays. , 2010, , .		1
197	Buffer management for multi-application image processing on multi-core platforms: Analysis and case study. , 2010, , .		1
198	Automated generation of an efficient MPEG-4 Reconfigurable Video Coding decoder implementation. , 2010, , .		1

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199	Modeling and optimization of dynamic signal processing in resource-aware sensor networks. , 2011, , .		1
200	A design tool for efficient mapping of multimedia applications onto heterogeneous platforms. , 2011, , .		1
201	Instrumentation-driven model detection for dataflow graphs. , 2012, , .		1
202	Parameterized Scheduling of Topological Patterns in Signal Processing Dataflow Graphs. Journal of Signal Processing Systems, 2013, 71, 275-286.	1.4	1
203	Dataflow modeling and design for cognitive radio networks. , 2013, , .		1
204	Subcarrier allocation and power control with LTE-A carrier aggregation. , 2013, , .		1
205	Data flow algorithms for processors with vector extensions: Handling actors with internal state. , 2014, , .		1
206	Partial expansion of dataflow graphs for resource-aware scheduling of multicore signal processing systems. , 2014, , .		1
207	Dynamic, data-driven spectrum management in cognitive small cell networks. , 2014, , .		1
208	Mapping Parameterized Dataflow Graphs onto FPGA Platforms. Academic Press Library in Signal Processing, 2014, 4, 643-673.	0.8	1
209	An efficient GPU implementation of a multirate resampler for multi-carrier systems. , 2015, , .		1
210	Low power design methodology for signal processing systems using lightweight dataflow techniques. , 2016, , .		1
211	Power and Thermal Modeling for Communication Systems. , 2016, , .		1
212	Jitter measurement on deep waveforms with constant memory. , 2016, , .		1
213	Data Flow Algorithms for Processors with Vector Extensions. Journal of Signal Processing Systems, 2017, 87, 21-31.	1.4	1
214	Low-power heterogeneous computing via adaptive execution of dataflow actors. , 2017, , .		1
215	A design tool for high performance image processing on multicore platforms. , 2018, , .		1
216	Model-Based Representations for Dataflow Schedules. Lecture Notes in Computer Science, 2018, , 88-105.	1.0	1

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217	Optimized implementation of digital signal processing applications with gapless data acquisition. Eurasip Journal on Advances in Signal Processing, 2019, 2019, .	1.0	1
218	Low Resolution Recognition of Aerial Images. , 2019, , .		1
219	Efficient Model Solving for Markov Decision Processes. , 2020, , .		1
220	Decidable Variable-Rate Dataflow for Heterogeneous Signal Processing Systems. , 2020, , .		1
221	Software synthesis from dataflow schedule graphs. SN Applied Sciences, 2021, 3, 1.	1.5	1
222	WGEVIA: A Graph Level Embedding Method for Microcircuit Data. Frontiers in Computational Neuroscience, 2020, 14, 603765.	1.2	1
223	Validation of object detection in UAV-based images using synthetic data. , 2021, , .		1
224	Feature Extraction and Classification for Communication Channels in Wireless Mechatronic Systems. , 2021, , .		1
225	Rapid Quality Assessment of Nonrigid Image Registration Based on Supervised Learning. Journal of Digital Imaging, 2021, 34, 1376.	1.6	1
226	Dynamic, Data-Driven Hyperspectral Image Classification on Resource-Constrained Platforms. Lecture Notes in Computer Science, 2020, , 320-327.	1.0	1
227	High-Level Synthesis of DSP Applications Using Adaptive Negative Cycle Detection. Eurasip Journal on Advances in Signal Processing, 2002, 2002, 1.	1.0	0
228	Design Methods for DSP Systems. Eurasip Journal on Advances in Signal Processing, 2006, 2006, 1.	1.0	0
229	Design and implementation of a device network application for distributed line-crossing recognition. , 2007, , .		0
230	Embedded Digital Signal Processing Systems. Eurasip Journal on Embedded Systems, 2007, 2007, 1-1.	1.2	0
231	Introduction to the Special Issue on Embedded Computing Systems for DSP. Journal of Signal Processing Systems, 2008, 50, 97-98.	1.4	0
232	Model-based mapping of a nonrigid image registration algorithm to heterogeneous architectures. , 2008, , .		0
233	Special Issue on Selected Papers from BiOCAS 2008 Guest Editors' Introduction. IEEE Transactions on Biomedical Circuits and Systems, 2009, 3, 361-362.	2.7	0
234	Teaching cross-platform design and testing methods for embedded systems using DICE. , 2011, , .		0

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235	Systematic integration of flowgraph- and module-level parallelism in implementation of DSP applications on multiprocessor systems-on-chip. , 2012, , .		0
236	Prototyping scalable digital signal processing systems for radio astronomy using dataflow models. Radio Science, 2012, 47, n/a-n/a.	0.8	0
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