

Chong-Min Kyung

List of Publications by Year in descending order

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Version: 2024-02-01

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papers

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24
all docs

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docs citations

24
times ranked

179
citing authors

#	ARTICLE	IF	CITATIONS
1	Unsupervised deep learning for depth estimation with offset pixels. Optics Express, 2020, 28, 8619.	3.4	1
2	Intensity guided cost metric for fast stereo matching under radiometric variations. Optics Express, 2018, 26, 4096.	3.4	15
3	Depth extraction using adaptive blur channel selection for dual aperture camera. , 2016, , .		0
4	A Content-Aware Video Encoding Scheme Based on Single-Pass Consistent Quality Control. IEEE Transactions on Broadcasting, 2016, 62, 800-816.	3.2	7
5	Memory-efficient background subtraction for battery-operated surveillance system. , 2014, , .		0
6	Runtime 3-D stacked cache data management for energy minimization of 3-D chip-multiprocessors. , 2014, , .		2
7	Exploring hybrid SRAM/MRAM L2 NUCA stacked on 3D chip-multiprocessors. , 2014, , .		0
8	Energy-Aware Operation of Black Box Surveillance Cameras under Event Uncertainty and Memory Constraint. , 2012, , .		5
9	Energy Awareness in Video Codec Design. , 2011, , 119-148.		0
10	A Dynamic Search Range Algorithm for Stabilized Reduction of Memory Traffic in Video Encoder. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1041-1046.	8.3	6
11	Low latency variable length coding scheme for frame memory recompression. , 2010, , .		6
12	A Multitransform Architecture for H.264/AVC High-Profile Coders. IEEE Transactions on Multimedia, 2010, 12, 157-167.	7.2	32
13	A Lossless Embedded Compression Using Significant Bit Truncation for HD Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 848-860.	8.3	76
14	A lossless embedded compression algorithm for high definition video coding. , 2009, , .		22
15	Lossless frame memory recompression for video codec preserving random accessibility of coding unit. IEEE Transactions on Consumer Electronics, 2009, 55, 2105-2113.	3.6	23
16	A High-Performance 2-D Inverse Transform Architecture for the H.264/AVC Decoder. , 2007, , .		8
17	Exploiting intellectual properties with imprecise design costs for system-on-chip synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 240-252.	3.1	6
18	MetaCore: an application-specific programmable DSP development system. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 173-183.	3.1	17

#	ARTICLE	IF	CITATIONS
19	Synthesis of application specific instructions for embedded DSP software. IEEE Transactions on Computers, 1999, 48, 603-614.	3.4	52
20	MDSP-II: a 16-bit DSP with mobile communication accelerator. IEEE Journal of Solid-State Circuits, 1999, 34, 397-404.	5.4	13
21	Digital signal processor with efficient RGB interpolation and histogram accumulation. IEEE Transactions on Consumer Electronics, 1998, 44, 1389-1395.	3.6	18
22	MetaCore. , 1998, , .		16
23	Multiple behavior module synthesis based on selective groupings. , 0, , .		1
24	Exploiting intellectual properties in ASIP designs for embedded DSP software. , 0, , .		3