Elad Alon

List of Publications by Year
in descending order

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94 papers	4,729 citations	172457 29 h-index	144013 57 g-index
94 all docs	94 docs citations	94 times ranked	4413 citing authors

#	Article	IF	Citations
1	An Output Bandwidth Optimized 200-Gb/s PAM-4 100-Gb/s NRZ Transmitter With 5-Tap FFE in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 21-31.	5.4	11
2	An Eight-Core 1.44-GHz RISC-V Vector Processor in 16-nm FinFET. IEEE Journal of Solid-State Circuits, 2022, 57, 140-152.	5.4	5
3	LAYGO: A Template-and-Grid-Based Layout Generation Engine for Advanced CMOS Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1012-1022.	5.4	19
4	A 71-to-86-GHz 16-Element by 16-Beam Multi-User Beamforming Integrated Receiver Sub-Array for Massive MIMO. IEEE Journal of Solid-State Circuits, 2021, 56, 3811-3826.	5.4	10
5	A 16mm² 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET. , 2021, , .		6
6	System Integration of RISC-V Processors with FD-SOI. Integrated Circuits and Systems, 2020, , 263-302.	0.2	0
7	A Mixed-Signal RISC-V Signal Analysis SoC Generator With a 16-nm FinFET Instance. IEEE Journal of Solid-State Circuits, 2019, 54, 2786-2801.	5.4	11
8	Open-Source EDA Tools and IP, A View from the Trenches. , 2019, , .		5
9	A Real-Time, 1.89-GHz Bandwidth, 175-kHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET. IEEE Journal of Solid-State Circuits, 2019, 54, 1993-2008.	5.4	5
10	Design and Automatic Generation of High-Speed Circuits for Wireline Communications. , 2019, , .		0
11	A 2-tap switched capacitor FFE transmitter achieving 1-20 Gb/s at 0.72-0.62 pJ/bit. , 2019, , .		0
12	A 65-nm CMOS I/Q RF Power DAC With 24- to 42-dB Third-Harmonic Cancellation and Up to 18-dB Mixed-Signal Filtering. IEEE Journal of Solid-State Circuits, 2018, 53, 1127-1138.	5.4	12
13	A 0.25â€“1.7-GHz, 3.9â€“13.7-mW Power-Scalable, â^10-dBm Harmonic Blocker-Tolerant Mixer-First RF-to-Digital Receiver for Massive MIMO Applications. IEEE Solid-State Circuits Letters, 2018, 1, 38-41.	2.0	6
14	A 2.7-mu W Neuromodulation AFE With 200 mV_{pp} Differential-Mode Stimulus Artifact Canceler Including On-Chip LMS Adaptation. IEEE Solid-State Circuits Letters, 2018, 1, 194-197.	2.0	9
15	An Automated SerDes Frontend Generator Verified With a 16-nm Instance Achieving 15 Gb/s at 1.96 pJ/bit. IEEE Solid-State Circuits Letters, 2018, 1, 245-248.	2.0	5
16	An Automated SerDes Frontend Generator Verified with a 16NM Instance Achieving 15 GB/S at 1.96 PJ/Bit. , 2018, , .		4
17	Generating the Next Wave of Custom Silicon. , 2018, , .		9
18	A Real-Time, Analog/Digital Co-Designed 1.89-GHz Bandwidth, 175-kHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET. , 2018, , .		4

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19	BAG2: A process-portable framework for generator-based AMS circuit design. , 2018, , .		73
20	A 0.4-to-4-GHz All-Digital RF Transmitter Package With a Band-Selecting Interposer Combining Three Wideband CMOS Transmitters. IEEE Transactions on Microwave Theory and Techniques, 2018, , 1-18.	4.6	3
21	A RISC-V Processor SoC With Integrated Power Management at Submicrosecond Timescales in 28 nm FD-SOI. IEEE Journal of Solid-State Circuits, 2017, 52, 1863-1875.	5.4	32
22	Analysis and Design of Integrated Active Cancellation Transceiver for Frequency Division Duplex Systems. IEEE Journal of Solid-State Circuits, 2017, 52, 2038-2054.	5.4	38
23	A 65-nm CMOS Wideband TDD Front-End With Integrated T/R Switching via PA Re-Use. IEEE Journal of Solid-State Circuits, 2017, 52, 1768-1782.	5.4	8
24	Reliable Next-Generation Cortical Interfaces for Chronic Brainâ€“Machine Interfaces and Neuroscience. Proceedings of the IEEE, 2017, 105, 73-82.	21.3	44
25	Design Techniques for a 60-Gb/s 288-mW NRZ Transceiver With Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2017, 52, 3474-3485.	5.4	29
26	A Wideband All-Digital CMOS RF Transmitter on HDI Interposers With High Power and Efficiency. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 4724-4743.	4.6	11
27	A 0.37mm2 LTE/Wi-Fi compatible, memory-based, runtime-reconfigurable 2n3m5k FFT accelerator integrated with a RISC-V core in 16nm FinFET. , 2017, , .		3
28	Blind parallel interrogation of ultrasonic neural dust motes based on canonical polyadic decomposition: A simulation study. , 2017, , .		0
29	Wireless Recording in the Peripheral Nervous System with Ultrasonic Neural Dust. Neuron, 2016, 91, 529-539.	8.1	417
30	A 65nm CMOS wideband TDD front-end with integrated T/R switching via PA re-use. , 2016, , .		2
31	Fully Inkjetâ€Printed Stressâ€Tolerant Microelectromechanical Reed Relays for Largeâ€Area Electronics. Advanced Electronic Materials, 2016, 2, 1500482.	5.1	12
32	An Agile Approach to Building RISC-V Microprocessors. IEEE Micro, 2016, 36, 8-20.	1.8	79
33	Design Techniques for a 60 Gb/s 173 mW Wireline Receiver Frontend in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2016, 51, 871-880.	5.4	22
34	Miniaturizing Ultrasonic System for Portable Health Care and Fitness. IEEE Transactions on Biomedical Circuits and Systems, 2016, 9, 1-1.	4.0	29
35	A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DCâ€“DC Converters in 28 nm FDSOI. IEEE Journal of Solid-State Circuits, 2016, 51, 930-942.	5.4	47
36	Ultrasonic beamforming system for interrogating multiple implantable sensors. , 2015, 2015, 2673-6.		13

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37	Specialization for energy efficiency using agile development. , 2015, , .		0
38	A 4.78 mm 2 Fully-Integrated Neuromodulation SoC Combining 64 Acquisition Channels With Digital Compression and Simultaneous Dual Stimulation. IEEE Journal of Solid-State Circuits, 2015, 50, 1038-1047.	5.4	75
39	Introduction to the Special Issue on the IEEE 2014 Custom Integrated Circuits Conference. IEEE Journal of Solid-State Circuits, 2015, 50, 1739-1740.	5.4	0
40	Dual-Input Switched Capacitor Converter Suitable for Wide Voltage Gain Range. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 413-420.	3.6	8
41	A RISC-V vector processor with tightly-integrated switched-capacitor DC-DC converters in 28nm FDSOI. , 2015, , .		24
42	A Minimally Invasive 64-Channel Wireless Î¼ECoG Implant. IEEE Journal of Solid-State Circuits, 2015, 50, 344-359.	5.4	295
43	Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 723-730.	3.1	38
44	Model validation of untethered, ultrasonic neural dust motes for cortical recording. Journal of Neuroscience Methods, 2015, 244, 114-122.	2.5	140
45	Exploitation of the coffee-ring effect to realize mechanically enhanced inkjet-printed microelectromechanical relays with U-bar-shaped cantilevers. Applied Physics Letters, 2014, 105, .	3.3	17
46	Beamforming approaches for untethered, ultrasonic neural dust motes for cortical recording: A simulation study. , 2014, 2014, 2625-8.		11
47	Design Techniques for a Mixed-Signal I/Q 32-Coefficient Rx-Feedforward Equalizer, 100-Coefficient Decision Feedback Equalizer in an 8 Gb/s 60 GHz 65 nm LP CMOS Receiver. IEEE Journal of Solid-State Circuits, 2014, 49, 2588-2607.	5.4	13
48	A 12.8 GS/s Time-Interleaved ADC With 25 GHz Effective Resolution Bandwidth and 4.6 ENOB. IEEE Journal of Solid-State Circuits, 2014, 49, 1725-1738.	5.4	34
49	Fully Integrated Switched-Capacitor DC-DC Conversion. , 2014, , 129-146.		0
50	The Road to Fully Integrated DCâ€“DC Conversion via the Switched-Capacitor Approach. IEEE Transactions on Power Electronics, 2013, 28, 4146-4155.	7.9	269
51	A 12.8GS/s time-interleaved SAR ADC with 25GHz 3dB ERBW and 4.6b ENOB. , 2013, , .		3
52	A Fully-Integrated, Miniaturized (0.125 mmÂ²) 10.5 ÂµW Wireless Neural Sensor. IEEE Journal of Solid-State Circuits, 2013, 48, 960-970.	5.4	154
53	A mixed-signal 32-coefficient RX-FFE 100-coefficient DFE for an 8Gb/s 60GHz receiver in 65nm LP CMOS. , 2013, , .		5
54	Design Considerations for a Direct Digitally Modulated WLAN Transmitter With Integrated Phase Path and Dynamic Impedance Modulation. IEEE Journal of Solid-State Circuits, 2013, 48, 3160-3177.	5.4	91

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55	A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm² at 73% efficiency. , 2013, , .		31
56	Design Techniques for a 66 Gb/s 46 mW 3-Tap Decision Feedback Equalizer in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 3243-3257.	5.4	28
57	A digitally modulated 2.4GHz WLAN transmitter with integrated phase path and dynamic load modulation in 65nm CMOS. , 2013, , .		22
58	A 66Gb/s 46mW 3-tap decision-feedback equalizer in 65nm CMOS. , 2013, , .		6
59	A 78-microwatt GSM phase noise-compliant pierce oscillator referenced to a 61-MHz wine-glass disk resonator. , 2013, , .		15
60	Physical principles for scalable neural recording. Frontiers in Computational Neuroscience, 2013, 7, 137.	2.1	215
61	Vibration-insensitive 61-MHz micromechanical disk reference oscillator. , 2012, , .		5
62	Recent progress and challenges for relay logic switch technology. , 2012, , .		8
63	A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication. , 2012, , .		154
64	10-Gbps, 5.3-mW Optical Transmitter and Receiver Circuits in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 2049-2067.	5.4	144
65	A 10Gb/s 10mW 2-tap reconfigurable pre-emphasis transmitter in 65nm LP CMOS. , 2012, , .		3
66	Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits. IEEE Electron Device Letters, 2012, 33, 281-283.	3.9	15
67	A Fully Integrated, 290 pJ/bit UWB Dual-Mode Transceiver for cm-Range Wireless Interconnects. IEEE Journal of Solid-State Circuits, 2012, 47, 586-598.	5.4	30
68	A 10 Gb/s 45 mW Adaptive 60 GHz Baseband in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 952-968.	5.4	42
69	A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters. IEEE Journal of Solid-State Circuits, 2012, 47, 1113-1122.	5.4	80
70	Design Requirements for Steeply Switching Logic Devices. IEEE Transactions on Electron Devices, 2012, 59, 326-334.	3.0	21
71	Digitally-assisted analog circuits for a 10 Gbps, 395 fJ/b optical receiver in 40 nm CMOS. , 2011, , .		5
72	Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver. Optics Express, 2011, 19, 5172.	3.4	138

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73	A multi-GHz area-efficient comparator with dynamic offset cancellation. , 2011, , .		11
74	Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters. IEEE Journal of Solid-State Circuits, 2011, 46, 2120-2131.	5.4	363
75	A 65 nm CMOS 4-Element Sub-34 mW/Element 60 GHz Phased-Array Transceiver. IEEE Journal of Solid-State Circuits, 2011, 46, 3018-3032.	5.4	114
76	An Efficient Mixed-Signal 2.4-GHz Polar Power Amplifier in 65-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2011, 46, 1796-1809.	5.4	142
77	Mechanical Computing Redux: Relays for Integrated Circuit Applications. Proceedings of the IEEE, 2010, 98, 2076-2094.	21.3	119
78	Prospects for MEM logic switch technology. , 2010, , .		16
79	Perfectly Complementary Relay Design for Digital Logic Applications. IEEE Electron Device Letters, 2010, 31, 371-373.	3.9	40
80	Optical Interconnect for High-End Computer Systems. IEEE Design and Test of Computers, 2010, 27, 10-19.	1.0	7
81	A sub-picojoule-per-bit CMOS photonic receiver for densely integrated systems. Optics Express, 2010, 18, 204.	3.4	59
82	Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications. , 2010, , .		45
83	A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm² at 81% efficiency. , 2010, , .		42
84	Clocking Links in Multi-chip Packages: A Case Study. , 2010, , .		1
85	Seesaw Relay Logic and Memory Circuits. Journal of Microelectromechanical Systems, 2010, 19, 1012-1014.	2.5	35
86	Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits. IEEE Electron Device Letters, 2010, 31, 890-892.	3.9	21
87	A 90 nm CMOS Low-Power 60 GHz Transceiver With Integrated Baseband Circuitry. IEEE Journal of Solid-State Circuits, 2009, 44, 3434-3447.	5.4	327
88	On-Die Power Supply Noise Measurement Techniques. IEEE Transactions on Advanced Packaging, 2009, 32, 248-259.	1.6	12
89	Design and reliability of a micro-relay technology for zero-standby-power digital logic applications. , 2009, , .		77
90	Energyâ€“Performance Tunable Logic. IEEE Journal of Solid-State Circuits, 2009, 44, 2554-2567.	5.4	5

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91	Digital Circuit Design Trends. IEEE Journal of Solid-State Circuits, 2008, 43, 757-761.	5.4	18
92	Integrated Regulation for Energy-Efficient Digital Circuits. IEEE Journal of Solid-State Circuits, 2008, 43, 1795-1807.	5.4	46
93	Integrated circuit design with NEM relays. , 2008, , .		103
94	Integrated Regulation for Energy-Efficient Digital Circuits. , 2007, , .		4