Pascal Meinerzhagen

List of Publications by Year
in descending order

26 papers	401 citations	1040056 9 h-index	1372567 10 g-index
26 all docs	26 docs citations	26 times ranked	307 citing authors

#	Article	IF	Citations
1	Energy/Reliability Trade-Offs in Low-Voltage ReRAM-Based Non-Volatile Flip-Flop Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3155-3164.	5.4	60
2	Benchmarking of Standard-Cell Based Memories in the Sub-$V_{m T}$ Domain in 65-nm CMOS Technology. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 173-182.	3.6	54
3	Exploration of Sub-VT and Near-VT 2T Gain-Cell Memories for Ultra-Low Power Applications under Technology Scaling. Journal of Low Power Electronics and Applications, 2013, 3, 54-72.	2.0	37
4	Single-Supply 3T Gain-Cell for Low-Voltage Low-Power Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 358-362.	3.1	33
5	Review and classification of gain cell eDRAM implementations. , 2012, , .		26
6	Replica Technique for Adaptive Refresh Timing of Gain-Cell-Embedded DRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 259-263.	3.0	24
7	Energy versus Data Integrity Trade-Offs in Embedded High-Density Logic Compatible Dynamic Memories. , 2015, , .		21
8	4T Gain-Cell with internal-feedback for ultra-low retention power at scaled CMOS nodes. , 2014, , .		19
9	Ultra Low Voltage Synthesizable Memories: A Trade-Off Discussion in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 806-817.	5.4	18
10	A 500 fW/bit 14 fJ/bit-access 4kb standard-cell based sub-V_T memory in 65nm CMOS. , 2012, , .		16
11	Silicon-Proven, Per-Cell Retention Time Distribution Model for Gain-Cell Based eDRAMs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 222-232.	5.4	15
12	Two-port low-power gain-cell storage array: Voltage scaling and retention time. , 2012, , .		11
13	Impact of body biasing on the retention time of gainâ€cell memories. Journal of Engineering, 2013, 2013, 19-22.	1.1	11
14	A sub-V<inf>T</inf> 2T gain-cell memory for biomedical applications. , 2012, , .		10
15	Analysis of Neutron-Induced Multibit-Upset Clusters in a 14-nm Flip-Flop Array. IEEE Transactions on Nuclear Science, 2019, 66, 918-925.	2.0	9
16	Hybrid GC-eDRAM/SRAM Bitcell for Robust Low-Power Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1362-1366.	3.0	8
17	TamaRISC-CS: An ultra-low-power application-specific processor for compressed sensing. , 2012, , .		7
18	TamaRISC-CS: An ultra-low-power application-specific processor for compressed sensing. , 2012, , .		5

#	Article	IF	Citations
19	A 35 fJ/bit-access sub-V<inf>T</inf> memory using a dual-bit area-optimized standard-cell in 65 nm CMOS. , 2014, , .		5
20	Refresh-free dynamic standard-cell based memories: Application to a QC-LDPC decoder. , 2015, , .		5
21	An ultra-dense irradiation test structure with a NAND/NOR readout chain for characterizing soft error rates of 14nm combinational logic circuits. , 2017, , .		5
22	A process compensated gain cell embedded-DRAM for ultra-low-power variation-aware design. , 2016, , .		1
23	Gain-Cell eDRAMs (GC-eDRAMs): Review of Basics and Prior Art. , 2018, , 13-26.		1
24	Retention Time Modeling: The Key to Low-Power GC-eDRAMs. , 2018, , 27-48.		0
25	Novel Bitcells for Scaled CMOS Nodes and Soft Error Tolerance. , 2018, , 113-134.		0
26	Novel Bitcells and Assist Techniques for NTV GC-eDRAMs. , 2018, , 61-90.		0