Qiang Xu

List of Publications by Year
in descending order

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96	1,962	840776 11	794594 19
papers	citations	h-index	g-index

96	96	96	1263
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	On Functional Test Generation for Deep Neural Network IPs. , 2019, , .		6
2	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	2.7	42
3	Shadow Block: Accelerating ORAM Accesses with Data Duplication. , 2018, , .		13
4	Lookup table allocation for approximate computing with memory under quality constraints. , 2018, , .		2
5	On efficient message passing in energy harvesting based distributed system. , 2017, , .		2
6	Low-overhead implementation of logic encryption using gate replacement techniques. , 2017, , .		9
7	ApproxQA: A unified quality assurance framework for approximate computing. , 2017, , .		3
8	ApproxLUT: A novel approximate lookup table-based accelerator. , 2017, , .		10
9	Fault injection attack on deep neural network. , 2017, , .		120
10	On Effective and Efficient Quality Management for Approximate Computing. , 2016, , .		18
11	SlideAcross: A Low-Latency Adaptive Router for Chip Multi-processor. , 2016, , .		3
12	Guest Editors' Introduction: Approximate Computing. IEEE Design and Test, 2016, 33, 6-7.	1.2	1
13	Approximate Computing: A Survey. IEEE Design and Test, 2016, 33, 8-22.	1.2	407
14	ApproxANN: An Approximate Computing Framework for Artificial Neural Network. , 2015, , .		114
15	On the Premises and Prospects of Timing Speculation. , 2015, , .		6
16	Vulnerability analysis for crypto devices against probing attack. , 2015, , .		0
17	ApproxIt: An approximate computing framework for iterative methods. , 2014, , .		4
18	On Trojan side channel design and identification. , 2014, , .		10

#	Article	IF	Citations
19	On the simulation of NBTI-Induced performance degradation considering arbitrary temperature and voltage variations. , 2014, , .		0
20	Energy-Efficient Design Techniques. , 2014, , 99-136.		2
21	On reconfiguration-oriented approximate adder design and its application. , 2013, , .		175
22	On Effective Through-Silicon Via Repair for 3-D-Stacked ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 559-571.	2.7	62
23	Optimization for timing-speculated circuits by redundancy addition and removal. , 2013, , .		1
24	On Multiplexed Signal Tracing for Post-Silicon Validation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 748-759.	2.7	8
25	ForTER: A forward error correction scheme for timing error resilience. , 2013, , .		5
26	On hardware Trojan design and implementation at register-transfer level. , 2013, , .		32
27	Path delay testing in resilient system. , 2013, , .		6
28	Clock skew scheduling for timing speculation. , 2012, , .		0
29	On effective TSV repair for 3D-stacked ICs. , 2012, , .		55
30	On Signal Selection for Visibility Enhancement in Trace-Based Post-Silicon Validation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1263-1274.	2.7	53
31	On modeling faults in FinFET logic circuits. , 2012, , .		42
32	On efficient silicon debug with flexible trace interconnection fabric. , 2012, , .		3
33	Learning-based power management for multi-core processors via idle period manipulation. , 2012, , .		3
34	CODA: A concurrent online delay measurement architecture for critical paths. , 2012, , .		4
35	On X-Variable Filling and Flipping for Capture-Power Reduction in Linear Decompressor-Based Test Compression Environment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1743-1753.	2.7	13
36	Yield enhancement for 3D-stacked ICs: Recent advances and challenges. , 2012, , .		25

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37	On Task Allocation and Scheduling for Lifetime Extension of Platform-Based MPSoC Designs. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 2088-2099.	5.6	55
38	Online clock skew tuning for timing speculation. , 2011, , .		13
39	Pseudo-functional testing for small delay defects considering power supply noise effects. , 2011, , .		10
40	On High-Quality Test Pattern Selection and Manipulation. , 2011, , .		0
41	On Timing Yield Improvement for FPGA Designs Using Architectural Symmetry. , 2011, , .		0
42	Compression-aware capture power reduction for at-speed testing. , 2011, , .		0
43	On multiplexed signal tracing for post-silicon debug. , 2011, , .		4
44	Lifetime Reliability for Load-Sharing Redundant Systems With Arbitrary Failure Distributions. IEEE Transactions on Reliability, 2010, 59, 319-330.	4.6	59
45	Energy-efficient task allocation and scheduling for multi-mode MPSoCs under lifetime reliability constraint. , 2010, , .		11
46	Yield enhancement for 3D-stacked memory by redundancy sharing across dies. , 2010, , .		41
47	Characterizing the lifetime reliability of manycore processors with core-level redundancy. , 2010, , .		18
48	Layout-aware pseudo-functional testing for critical paths considering power supply noise effects. , 2010, , .		2
49	On timing-independent false path identification. , 2010, , .		3
50	An FPGA chip identification generator using configurable ring oscillator. , 2010, , .		3
51	Modeling TSV open defects in 3D-stacked DRAM. , 2010, , .		22
52	X-Filling for Simultaneous Shift- and Capture-Power Reduction in At-Speed Scan-Based Testing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1081-1092.	3.1	21
53	Economic Analysis of Testing Homogeneous Manycore Chips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1257-1270.	2.7	3
54	AgeSim: A simulation framework for evaluating the lifetime reliability of processor-based SoCs. , 2010, , .		7

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55	On signal tracing in post-silicon validation. , 2010, , .		19
56	Fine-grained characterization of process variation in FPGAs. , 2010, , .		21
57	Lifetime reliability-aware task allocation and scheduling for MPSoC platforms. , 2009, , .		17
58	Trace signal selection for debugging electrical errors in post-silicon validation. , 2009, , .		3
59	On simultaneous shift- and capture-power reduction in linear decompressor-based test compression environment. , 2009, , .		27
60	A generic framework for scan capture power reduction in fixed-length symbol-based test compression environment. , 2009, , .		0
61	On Topology Reconfiguration for Defect-Tolerant NoC-Based Homogeneous Manycore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1173-1186.	3.1	70
62	Test architecture design and optimization for three-dimensional SoCs. , 2009, , .		54
63	Trace signal selection for visibility enhancement in post-silicon validation. , 2009, , .		2
64	Test economics for homogeneous manycore systems. , 2009, , .		4
65	Compression-aware pseudo-functional testing. , 2009, , .		6
66	Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks. , 2009, , .		0
67	Low-Power Scan Testing for Test Data Compression Using a Routing-Driven Scan Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1101-1105.	2.7	20
68	A debug probe for concurrently debugging multiple embedded cores and inter-core transactions in NoC-based systems. , 2008, , .		0
69	On capture power-aware test data compression for scan-based testing. , 2008, , .		0
70	Channel Width Utilization Improvement in Testing NoC-Based Systems for Test Time Reduction. , 2008, , .		6
71	On Modeling the Lifetime Reliability of Homogeneous Manycore Systems. , 2008, , .		13
72	A Generic Framework for Scan Capture Power Reduction in Test Compression Environment. , 2008, , .		2

#	Article	IF	Citations
73	Is It Cost-Effective to Achieve Very High Fault Coverage for Testing Homogeneous SoCs with Core-Level Redundancy?. , 2008, , .		1
74	Re-Examining the Use of Network-on-Chip as Test Access Mechanism. , 2008, , .		3
75	Defect Tolerance in Homogeneous Manycore Processors Using Core-Level Redundancy with Unified Topology. , 2008, , .		28
76	On Reusing Test Access Mechanisms for Debug Data Transfer in SoC Post-Silicon Validation. , 2008, , .		8
77	iFill: An Impact-Oriented X-Filling Method for Shift- and Capture-Power Reduction in At-Speed Scan-Based Testing. , 2008, , .		7
78	In-band Cross-Trigger Event Transmission for Transaction-Based Debug. , 2008, , .		4
79	On reducing both shift and capture power for scan-based testing. , 2008, , .		8
80	Pattern-directed circuit virtual partitioning for test power reduction. , 2007, , .		15
81	Test Wrapper Design and Optimization Under Power Constraints for Embedded Cores With Multiple Clock Domains. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1539-1547.	2.7	9
82	Test-wrapper designs for the detection of signal-integrity faults on core-external interconnects of SoCs. , 2007, , .		3
83	Test/Repair Area Overhead Reduction for Small Embedded SRAMs. Proceedings of the Asian Test Symposium, 2006, , .	0.0	10
84	Multifrequency TAM design for hierarchical SOCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 181-196.	2.7	2
85	DFT infrastructure for broadside two-pattern test of core-based SOCs. IEEE Transactions on Computers, 2006, 55, 470-485.	3.4	15
86	Wrapper design for multifrequency IP cores. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 678-685.	3.1	5
87	Modular and rapid testing of SOCs with unwrapped logic blocks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 1275-1285.	3.1	4
88	Hardware/software co-testing of embedded memories in complex SOCs. , 0, , .		1
89	Delay fault testing of core-based systems-on-a-chip. , 0, , .		1
90	On reducing wrapper boundary register cells in modular soc testing. , 0, , .		6

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91	Multi-Frequency Test Access Mechanism Design for Modular SOC Testing. , 0, , .		25
92	Time/area tradeoffs in testing hierarchical SOCs with hard mega-cores. , 0, , .		9
93	Wrapper design for testing IP cores with multiple clock domains. , 0, , .		1
94	Register-transfer level functional scan for hierarchical designs. , 0, , .		0
95	On concurrent test of wrapped cores and unwrapped logic blocks in SOCs. , 0, , .		2
96	Retention-Aware Test Scheduling for BISTed Embedded SRAMs. , 0, , .		0