Jun Lin

List of Publications by Year
in descending order

127	1,393	471509	477307
papers	citations	17 h-index	29 g-index

127	127	127	1108
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Efficient Software Implementation of the SIKE Protocol Using a New Data Representation. IEEE Transactions on Computers, 2022, 71, 670-683.	3.4	4
2	A Proximal Iteratively Reweighted Approach for Efficient Network Sparsification. IEEE Transactions on Computers, 2022, 71, 185-196.	3.4	1
3	Evaluations on Deep Neural Networks Training Using Posit Number System. IEEE Transactions on Computers, 2021, 70, 174-187.	3.4	30
4	Design of High-Performance and Area-Efficient Decoder for 5G LDPC Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 879-891.	5.4	17
5	Fast Modular Multipliers for Supersingular Isogeny-Based Post-Quantum Cryptography. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 359-371.	3.1	7
6	An Improved Reliability-Based Decoding Algorithm for NB-LDPC Codes. IEEE Communications Letters, 2021, 25, 1153-1157.	4.1	2
7	An Efficient and Flexible Accelerator Design for Sparse Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2936-2949.	5.4	27
8	Low-Latency Hardware Accelerator for Improved Engle-Granger Cointegration in Pairs Trading. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2911-2924.	5.4	5
9	Counter Random Gradient Descent Bit-Flipping Decoder for LDPC Codes. , 2021, , .		4
10	PipeBSW: A Two-Stage Pipeline Structure for Banded Smith-Waterman Algorithm on FPGA. , 2021, , .		3
11	An FPGA-Based Reconfigurable Accelerator for Low-Bit DNN Training. , 2021, , .		3
12	Automatic Generation of Dynamic Inference Architecture for Deep Neural Networks. , 2021, , .		0
13	Reducing Search Complexity of Dynamic SC-Flip Decoding for Polar Codes. , 2021, , .		0
14	Optimized Trellis-Based Min-Max Decoder for NB-LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 57-61.	3.0	9
15	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1399-1403.	3.0	3
16	Exploring Quantization in Few-Shot Learning. , 2020, , .		1
17	Information Storage Bit-Flipping Decoder for LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2464-2468.	3.1	9
18	A Serial Maximum-likelihood Detection Algorithm for Massive MIMO Systems. , 2020, , .		1

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19	Hardware Accelerator for Engle-Granger Cointegration in Pairs Trading. , 2020, , .		3
20	LSTM-Based Quantitative Trading Using Dynamic K-Top and Kelly Criterion. , 2020, , .		2
21	A Computation-Efficient Solution for Acceleration of Generative Adversarial Network. , 2020, , .		3
22	A Precision-Scalable Energy-Efficient Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3484-3497.	5.4	18
23	Fine-Grained Bit-Flipping Decoding for LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 896-900.	3.0	10
24	Efficient Precision-Adjustable Architecture for Softmax Function in Deep Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3382-3386.	3.0	29
25	Multi-Layer Generalized Integrated Interleaved Codes. IEEE Communications Letters, 2020, 24, 1880-1884.	4.1	4
26	Efficient FPGA design for Convolutions in CNN based on FFT-pruning. , 2020, , .		1
27	LBFP: Logarithmic Block Floating Point Arithmetic for Deep Neural Networks. , 2020, , .		4
28	A Configurable FPGA Accelerator of Bi-LSTM Inference with Structured Sparsity. , 2020, , .		3
29	Hardware Accelerator for Multi-Head Attention and Position-Wise Feed-Forward in the Transformer. , 2020, , .		35
30	A High-Speed Successive-Cancellation Decoder for Polar Codes Using Approximate Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 227-231.	3.0	6
31	FPAP: A Folded Architecture for Energy-Quality Scalable Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 288-301.	5.4	10
32	A New Clock Phase Calibration Method in High-Speed and High-Resolution DACs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 332-336.	3.0	0
33	An Efficient Post-Processor for Lowering the Error Floor of LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 397-401.	3.0	2
34	Background Calibration of Comparator Offsets in SHA-Less Pipelined ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 357-361.	3.0	4
35	A New Probabilistic Gradient Descent Bit Flipping Decoder for LDPC Codes. , 2019, , .		4
36	Methodology for Efficient Reconfigurable Architecture of Generative Neural Network. , 2019, , .		7

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37	TIE. , 2019, , .		38
38	A Novel Low-Complexity Joint Coding and Decoding Algorithm for NB-LDPC Codes. , 2019, , .		3
39	A New Fast-SSC-Flip Decoding of Polar Codes. , 2019, , .		5
40	A Hardware-Oriented and Memory-Efficient Method for CTC Decoding. IEEE Access, 2019, 7, 120681-120694.	4.2	5
41	USCA: A Unified Systolic Convolution Array Architecture for Accelerating Sparse Neural Network. , 2019, , .		10
42	Efficient T-EMS Based Decoding Algorithms for High-Order LDPC Codes. IEEE Access, 2019, 7, 50980-50992.	4.2	6
43	Improved Fast-SSC-Flip Decoding of Polar Codes. IEEE Communications Letters, 2019, 23, 950-953.	4.1	12
44	A Low-latency Sparse-Winograd Accelerator for Convolutional Neural Networks. , 2019, , .		20
45	Analysis and Design of a Large Dither Injection Circuit for Improving Linearity in Pipelined ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2008-2020.	3.1	11
46	E-LSTM: An Efficient Hardware Architecture for Long Short-Term Memory. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 280-291.	3.6	41
47	A 124-Gb/s Decoder for Generalized Integrated Interleaved Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3174-3187.	5.4	16
48	An Improved Gradient Descent Bit-Flipping Decoder for LDPC Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3188-3200.	5.4	18
49	Modified GII-BCH Codes for Low-Complexity and Low-Latency Encoders. IEEE Communications Letters, 2019, 23, 785-788.	4.1	7
50	Improved Soft-Assisted Iterative Bounded Distance Decoding for Product Codes. , 2019, , .		1
51	Redundancy-Aided Iterative Reliability-Based Majority-Logic Decoding for NB-LDPC Codes. , 2019, , .		0
52	DynExit: A Dynamic Early-Exit Strategy for Deep Residual Networks. , 2019, , .		15
53	Ultra-Fast Modular Multiplication Implementation for Isogeny-Based Post-Quantum Cryptography. , 2019, , .		7
54	A 100 Gbps Turbo Product Code Decoder for Optical Communications. , 2019, , .		3

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55	A Decomposition Mapping based Quantized Belief Propagation Decoding for 5G LDPC Codes. , 2019, , .		0
56	A Low-Latency and Low-Complexity Hardware Architecture for CTC Beam Search Decoding. , 2019, , .		1
57	An Enhanced Offset Min-Sum decoder for 5G LDPC Codes. , 2019, , .		0
58	EAGLE: Exploiting Essential Address in Both Weight and Activation to Accelerate CNN Computing. , 2019, , .		0
59	Training Deep Neural Networks Using Posit Number System. , 2019, , .		11
60	A Low-Complexity Error-and-Erasure Decoding Algorithm for t=2 RS Codes. , 2019, , .		3
61	Hybrid Preconditioned CG Detection with Sequential Update for Massive MIMO Systems. , 2019, , .		1
62	Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes. , 2019, , .		9
63	A Low-Complexity RS Decoder for Triple-Error-Correcting RS Codes. , 2019, , .		2
64	Fast-ABC: A Fast Architecture for Bottleneck-Like Based Convolutional Neural Networks. , 2019, , .		10
65	An Improved Gauss-Seidel Algorithm and Its Efficient Architecture for Massive MIMO Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1194-1198.	3.0	30
66	Efficient Hardware Architectures for Deep Convolutional Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1941-1953.	5.4	106
67	Low Complexity Message Passing Detection Algorithm for Large-Scale MIMO Systems. IEEE Wireless Communications Letters, 2018, 7, 708-711.	5.0	32
68	A Stage-Combined Belief Propagation Decoder for Polar Codes. Journal of Signal Processing Systems, 2018, 90, 687-694.	2.1	4
69	A 21.66 Gbps Nonbinary LDPC Decoder for High-Speed Communications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 226-230.	3.0	8
70	An Energy-Efficient Architecture for Binary Weight Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 280-293.	3.1	54
71	A High-Speed and Low-Complexity Architecture for Softmax Function in Deep Learning. , 2018, , .		74
72	A Low-Complexity Decoder for Turbo Product Codes Based on Extended Hamming Codes. , 2018, , .		5

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73	Comparison between Generalized Integrated Interleaved Codes and Generalized Error Location Codes. , 2018, , .		2
74	Efficient Reconfigurable Hardware Core for Convolutional Neural Networks. , 2018, , .		1
75	Fast and Low-Complexity Decoding Algorithm and Architecture for Quadruple-Error-Correcting RS codes. , 2018, , .		4
76	A Low-Complexity Massive MIMO Detection Algorithm Based on Matrix Partition. , 2018, , .		3
77	Analysis of the Dual-Threshold-Based Shrinking Scheme for Efficient NB-LDPC Decoding. , 2018, , .		0
78	A Novel Hardware Architecture to Accelerate Burrows-Wheeler Transform. , 2018, , .		1
79	Approximate Belief Propagation Decoder for Polar Codes. , 2018, , .		5
80	Approximate Comparator: Design and Analysis. , 2018, , .		6
81	Bandwidth Efficient Architectures for Convolutional Neural Network. , 2018, , .		0
82	A Novel Compiler for Regular Expression Matching Engine Construction. , 2018, , .		0
83	Increasing the Accuracy of Approximate Adders with Very Low Extra Complexity. , 2018, , .		0
84	Eadnet: Efficient Architecture for Decomposed Convolutional Neural Networks. , 2018, , .		0
85	An Efficient NB-LDPC Decoding Algorithm for Next-Generation Memories. , 2018, , .		2
86	A New Soft-input Hard-output decoding algorithm for Turbo Product Codes. , 2018, , .		1
87	Hardware-Oriented Compression of Long Short-Term Memory for Efficient Inference. IEEE Signal Processing Letters, 2018, 25, 984-988.	3.6	8
88	Parameter-Free <inline-formula> <tex-math notation="LaTeX">ell_p </tex-math> </inline-formula>-Box Decoding of LDPC Codes. IEEE Communications Letters, 2018, 22, 1318-1321.	4.1	8
89	An Efficient Convolution Core Architecture for Privacy-Preserving Deep Learning. , 2018, , .		11
90	FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks. , 2018, , .		2

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91	An Optimized Architecture For Decomposed Convolutional Neural Networks. , 2018, , .		0
92	Low-complexity detection algorithms based on matrix partition for massive MIMO. , 2017, , .		4
93	Accelerating Recurrent Neural Networks: A Memory-Efficient Approach. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2763-2775.	3.1	68
94	Efficient Soft Cancelation Decoder Architectures for Polar Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 87-99.	3.1	11
95	Energy efficient SVM classifier using approximate computing. , 2017, , .		6
96	Efficient approximate layered LDPC decoder. , 2017, , .		5
97	Reduced complexity message passing detection algorithm in large-scale MIMO systems. , 2017, , .		3
98	Reduced complexity list polar decoder with an improved path pruning scheme. , 2017, , .		0
99	A reduced complexity decoding algorithm for NB-LDPC codes. , 2017, , .		2
100	An access pattern based adaptive mapping function for GPGPU scratchpad memory. IEICE Electronics Express, 2017, 14, 20170373-20170373.	0.8	0
101	Optimized sorting network for successive cancellation list decoding of polar codes. IEICE Electronics Express, 2017, 14, 20170735-20170735.	0.8	5
102	An efficient post processing scheme to lower the error floor of LDPC decoders. , 2017, , .		1
103	Intra-layer nonuniform quantization of convolutional neural network. , 2016, , .		6
104	An Efficient Hardware Architecture for Lossless Data Compression in Data Center. , 2016, , .		1
105	Efficient convolution architectures for convolutional neural network. , 2016, , .		22
106	A Multimode Area-Efficient SCL Polar Decoder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3499-3512.	3.1	23
107	Error performance analysis of the symbol-decision SC polar decoder. , 2016, , .		0
108	An ultra-long FFT architecture implemented in a reconfigurable application specified processor. IEICE Electronics Express, 2016, 13, 20160504-20160504.	0.8	7

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109	Design and implementation of high performance matrix inversion based on reconfigurable processor. IEICE Electronics Express, 2016, 13, 20160579-20160579.	0.8	2
110	A high throughput belief propagation decoder architecture for polar codes. , 2016, , .		4
111	Efficient approximate ML decoding units for polar list decoders. , 2015, , .		0
112	A hybrid partial sum computation unit architecture for list decoders of polar codes. , 2015, , .		2
113	Reduced complexity belief propagation decoders for polar codes. , 2015, , .		17
114	An Efficient List Decoder Architecture for Polar Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2508-2518.	3.1	51
115	A High Throughput List Decoder Architecture for Polar Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-14.	3.1	24
116	A reduced latency list decoding algorithm for polar codes. , 2014, , .		23
117	Efficient Error Control Decoder Architectures for Noncoherent Random Linear Network Coding. Journal of Signal Processing Systems, 2014, 76, 195-209.	2.1	0
118	Efficient list decoder architecture for polar codes. , 2014, , .		23
119	An Efficient Fully Parallel Decoder Architecture for Nonbinary LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2649-2660.	3.1	14
120	Efficient Shuffled Decoder Architecture for Nonbinary Quasi-Cyclic LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1756-1761.	3.1	18
121	Linearized Polynomial Interpolation and Its Applications. IEEE Transactions on Signal Processing, 2013, 61, 206-217.	5.3	9
122	Modified shuffled schedule for nonbinary low-density parity-check codes. , 2012, , .		0
123	Reduced-Complexity Decoders of Long Reed-Solomon Codes Based on Composite Cyclotomic Fourier Transforms. IEEE Transactions on Signal Processing, 2012, 60, 3920-3925.	5.3	6
124	Flexible LDPC Decoder Design for Multigigabit-per-Second Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 116-124.	5.4	43
125	An Efficient VLSI Architecture for Nonbinary LDPC Decoders. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 51-55.	3.0	33
126	Efficient Decoder Design for Nonbinary Quasicyclic LDPC Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1071-1082.	5.4	61

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127	LDPC decoder design for high rate wireless personal area networks. IEEE Transactions on Consumer Electronics, 2009, 55, 455-460.	3.6	6