Andrew B Kahng

List of Publications by Year
in descending order

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59 papers	2,900 citations	471509 17 h-index	315739 38 g-index
59 all docs	59 docs citations	59 times ranked	1579 citing authors

#	Article	IF	Citations
1	Recent directions in netlist partitioning: a survey. The Integration VLSI Journal, 1995, 19, 1-81.	2.1	494
2	ORION 2.0: A fast and accurate NoC power and area model for early-stage design space exploration. , 2009, , .		456
3	A new adaptive multi-start technique for combinatorial global optimizations. Operations Research Letters, 1994, 16, 101-113.	0.7	312
4	ORION 2.0: A Power-Area Simulator for Interconnection Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 191-196.	3.1	218
5	Spectral partitioning with multiple eigenvectors. Discrete Applied Mathematics, 1999, 90, 3-26.	0.9	131
6	Power-aware placement. , 2005, , .		94
7	Robust IP watermarking methodologies for physical design. , 1998, , .		86
8	On switch factor based analysis of coupled RC interconnects. , 2000, , .		85
9	ORION3.0: A Comprehensive NoC Router Estimation Tool. IEEE Embedded Systems Letters, 2015, 7, 41-45.	1.9	83
10	Layout Decomposition Approaches for Double Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 939-952.	2.7	74
11	CMP Fill Synthesis: A Survey of Recent Studies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 3-19.	2.7	66
12	Old Bachelor Acceptance: A New Class of Non-Monotone Threshold Accepting Methods. ORSA Journal on Computing, 1995, 7, 417-425.	1.7	65
13	Machine Learning Applications in Physical Design. , 2018, , .		60
14	Sensitivity-guided metaheuristics for accurate discrete gate sizing. , 2012, , .		54
15	APlace. , 2005, , .		52
16	Scaling: More than Moore's law. IEEE Design and Test of Computers, 2010, 27, 86-87.	1.0	49
17	Accurate Machine-Learning-Based On-Chip Router Modeling. IEEE Embedded Systems Letters, 2010, 2, 62-66.	1.9	36
18	Enhancing the Efficiency of Energy-Constrained DVFS Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1769-1782.	3.1	35

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19	Improved Large-Step Markov Chain Variants for the Symmetric TSP. Journal of Heuristics, 1997, 3, 63-81.	1.4	28
20	New directions for learning-based IC design tools and methodologies. , 2018, , .		28
21	New efficient algorithms for computing effective capacitance. , 1998, , .		26
22	Best-so-far vs. where-you-are: implications for optimal finite-time annealing. Systems and Control Letters, 1994, 22, 71-78.	2.3	23
23	Match twice and stitch: a new TSP tour construction heuristic. Operations Research Letters, 2004, 32, 499-509.	0.7	23
24	Synthesis and Analysis of Design-Dependent Ring Oscillator (DDRO) Performance Monitors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2117-2130.	3.1	22
25	A DOE Set for Normalization-Based Extraction of Fill Impact on Capacitances. , 2007, , .		21
26	Adaptive Tuning of Photonic Devices in a Photonic NoC Through Dynamic Workload Allocation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 801-814.	2.7	20
27	Improved on-chip router analytical power and area modeling. , 2010, , .		19
28	Fast Dual-Graph-Based Hotspot Filtering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1635-1642.	2.7	18
29	Tuning Strategies for Global Interconnects in High-Performance Deep-Submicron ICs. VLSI Design, 1999, 10, 21-34.	0.5	17
30	Routing-aware scan chain ordering. ACM Transactions on Design Automation of Electronic Systems, 2005, 10, 546-560.	2.6	17
31	Timing Yield-Aware Color Reassignment and Detailed Placement Perturbation for Bimodal CD Distribution in Double Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1229-1242.	2.7	16
32	Fast and Efficient Bright-Field AAPSM Conflict Detection and Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 115-126.	2.7	13
33	Reducing time and effort in IC implementation: a roadmap of challenges and solutions. , 2018, , .		12
34	Statistical Timing Analysis in the Presence of Signal-Integrity Effects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1873-1877.	2.7	11
35	Scalable Heuristics for Design of DNA Probe Arrays. Journal of Computational Biology, 2004, 11, 429-447.	1.6	10
36	Quantifying Error in Dynamic Power Estimation of CMOS Circuits. Analog Integrated Circuits and Signal Processing, 2005, 42, 253-264.	1.4	10

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37	Accurate Predictive Interconnect Modeling for System-Level Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 679-684.	3.1	10
38	Enhancing sensitivity-based power reduction for an industry IC design context. The Integration VLSI Journal, 2019, 66, 96-111.	2.1	10
39	Revisiting inherent noise floors for interconnect prediction. , 2020, , .		10
40	OPTIMAL ALGORITHMS FOR SUBSTRATE TESTING IN MULTI-CHIP MODULES. International Journal of High Speed Electronics and Systems, 1995, 06, 595-612.	0.7	9
41	Impact of Adaptive Voltage Scaling on Aging-Aware Signoff. , 2013, , .		9
42	On Aging-Aware Signoff for Circuits With Adaptive Voltage Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2920-2930.	5.4	9
43	PROBE: A Placement, Routing, Back-End-of-Line Measurement Utility. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1459-1472.	2.7	8
44	Design technology productivity in the DSM era (invited talk). , 2001, , .		7
45	PROBE2.0: A Systematic Framework for Routability Assessment From Technology to Design in Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1495-1508.	2.7	7
46	TritonRoute-WXL: The Open-Source Router With Integrated DRC Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1076-1089.	2.7	7
47	Stochastic Power/Ground Supply Voltage Prediction and Optimization Via Analytical Placement. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 904-912.	3.1	6
48	DOE-Based Extraction of CMP, Active and Via Fill Impact on Capacitances. IEEE Transactions on Semiconductor Manufacturing, 2008, 21, 22-32.	1.7	5
49	Architectural-level prediction of interconnect wirelength and fanout. , 2009, , .		4
50	Benchmarking of Mask Fracturing Heuristics. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 170-183.	2.7	3
51	INVITED: Reducing Time and Effort in IC Implementation: A Roadmap of Challenges and Solutions. , 2018, , .		3
52	OPTIMAL ALGORITHMS FOR SUBSTRATE TESTING IN MULTI-CHIP MODULES. Selected Topics in Electornics and Systems, 1996, , 181-198.	0.2	3
53	Roads not taken. IEEE Design and Test of Computers, 2011, 28, 74-75.	1.0	2
54	COMPUTER-AIDED OPTIMIZATION OF DNA ARRAY DESIGN AND MANUFACTURING. , 2006, , 235-269.		1

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55	The Future of Signoff. IEEE Design and Test of Computers, 2011, 28, 86-89.	1.0	1
56	Toward Holistic Modeling, Margining and Tolerance of IC Variability. , 2014, , .		1
57	MILP-Based Optimization of 2-D Block Masks for Timing-Aware Dummy Segment Removal in Self-Aligned Multiple Patterning Layouts. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1075-1088.	2.7	1
58	How to test a tree. Networks, 1998, 32, 189-197.	2.7	0
59	Interconnect Matching Design Rule Inferring and Optimization through Correlation Extraction. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	0