Anand Raghunathan

List of Publications by Year
in descending order

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227	9,265	147726	123376
papers	citations	31 h-index	61 g-index

230	230	230	4925
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Ax-BxP: Approximate Blocked Computation for Precision-reconfigurable Deep Neural Network Acceleration. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-20.	1.9	2
2	RxNN: A Framework for Evaluating Deep Neural Networks on Resistive Crossbars. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 326-338.	1.9	54
3	Value Similarity Extensions for Approximate Computing in General-Purpose Processors. , 2021, , .		4
4	TxSim: Modeling Training of Deep Neural Networks on Resistive Crossbar Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 730-738.	2.1	21
5	Design Tools for Resistive Crossbar based Machine Learning Accelerators. , 2021, , .		2
6	Contention-aware Adaptive Model Selection for Machine Vision in Embedded Systems. , 2021, , .		1
7	Probabilistic Spike Propagation for Efficient Hardware Implementation of Spiking Neural Networks. Frontiers in Neuroscience, 2021, 15, 694402.	1.4	1
8	Efficacy of Pruning in Ultra-Low Precision DNNs. , 2021, , .		0
9	Accelerating DNN Training Through Selective Localized Learning. Frontiers in Neuroscience, 2021, 15, 759807.	1.4	2
10	PIM-DRAM: Accelerating Machine Learning Workloads Using Processing in Commodity DRAM. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 701-710.	2.7	6
11	Logic Synthesis of Approximate Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2503-2515.	1.9	16
12	Resistive Crossbars as Approximate Hardware Building Blocks for Machine Learning: Opportunities and Challenges. Proceedings of the IEEE, 2020, 108, 2276-2310.	16.4	55
13	Communication-efficient View-Pooling for Distributed Multi-View Neural Networks. , 2020, , .		4
14	Gradual Channel Pruning While Training Using Feature Relevance Scores for Convolutional Neural Networks. IEEE Access, 2020, 8, 171924-171932.	2.6	17
15	Sparsity Turns Adversarial: Energy and Latency Attacks on Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4129-4141.	1.9	4
16	Pruning Filters while Training for Efficiently Optimizing Deep Learning Networks. , 2020, , .		15
17	Sparsity-Aware Caches to Accelerate Deep Neural Networks. , 2020, , .		1
18	Emerging Neural Workloads and Their Impact on Hardware. , 2020, , .		4

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19	Ternary Compute-Enabled Memory using Ferroelectric Transistors for Accelerating Deep Neural Networks. , 2020, , .		5
20	Approximate Memory Compression. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 980-991.	2.1	11
21	Valley-Coupled-Spintronic Non-Volatile Memories With Compute-In-Memory Support. IEEE Nanotechnology Magazine, 2020, 19, 635-647.	1.1	7
22	TiM-DNN: Ternary In-Memory Accelerator for Deep Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1567-1577.	2.1	20
23	D <scp>y</scp> VED <scp>eep</scp>. Transactions on Embedded Computing Systems, 2020, 19, 1-24.	2.1	2
24	A Case for Generalizable DNN Cost Models for Mobile Devices. , 2020, , .		2
25	Data Subsetting: A Data-Centric Approach to Approximate Computing. , 2019, , .		4
26	X-MANN. , 2019, , .		20
27	Manna. , 2019, , .		15
28	Dynamic Spike Bundling for Energy-Efficient Spiking Neural Networks. , 2019, , .		15
29	Non-Volatile Memory utilizing Reconfigurable Ferroelectric Transistors to enable Differential Read and Energy-Efficient In-Memory Computation. , 2019, , .		16
30	Cache Memory Design With Magnetic Skyrmions in a Long Nanotrack. IEEE Transactions on Magnetics, 2019, 55, 1-9.	1.2	6
31	Pack and Detect. , 2019, , .		8
32	SparCE: Sparsity Aware General-Purpose Core Extensions to Accelerate Deep Neural Networks. IEEE Transactions on Computers, 2019, 68, 912-925.	2.4	19
33	Automatic Synthesis Techniques for Approximate Circuits. , 2019, , 123-140.		2
34	CxDNN. Transactions on Embedded Computing Systems, 2019, 18, 1-23.	2.1	40
35	Computing in Memory With Spin-Transfer Torque Magnetic RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 470-483.	2.1	235
36	Computing-in-memory with spintronics. , 2018, , .		12

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37	AxBA. , 2018, , .		19
38	ACCLIB: Accelerators as libraries. , 2018, , .		0
39	Energy Efficient Neural Computing: A Study of Cross-Layer Approximations. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 796-809.	2.7	32
40	Approximate Computing for Long Short Term Memory (LSTM) Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2266-2276.	1.9	36
41	A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensory Data Transfer. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 379-390.	2.7	4
42	Energy-Efficient Neural Computing with Approximate Multipliers. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-23.	1.8	57
43	SYNCVIBE: Fast and Secure Device Pairing through Physical Vibration on Commodity Smartphones. , 2018, , .		10
44	Model-based Iterative CT Image Reconstruction on GPUs. , 2017, , .		13
45	Wearable Medical Sensor-Based System Design: A Survey. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 124-138.	2.5	104
46	Approximate computing for spiking neural networks. , 2017, , .		32
47	A Pathway to Enable Exponential Scaling for the Beyond-CMOS Era. , 2017, , .		19
48	Energy-Efficient Object Detection Using Semantic Decomposition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2673-2677.	2.1	5
49	Approximate Error Detection With Stochastic Checkers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2258-2270.	2.1	3
50	Yield, Area, and Energy Optimization in STT-MRAMs Using Failure-Aware ECC. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-20.	1.8	6
51	ScaleDeep. Computer Architecture News, 2017, 45, 13-26.	2.5	23
52	AXSERBUS: A quality-configurable approximate serial bus for energy-efficient sensing. , 2017, , .		16
53	Model-based Iterative CT Image Reconstruction on GPUs. ACM SIGPLAN Notices, 2017, 52, 207-220.	0.2	10
54	ScaleDeep. , 2017, , .		122

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55	STAxCache: An approximate, energy efficient STT-MRAM cache. , 2017, , .		27
56	DISASTER: Dedicated Intelligent Security Attacks on Sensor-Triggered Emergency Responses. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 255-268.	2.5	9
57	CABA: Continuous Authentication Based on BioAura. IEEE Transactions on Computers, 2017, 66, 759-772.	2.4	48
58	Design and Management of Battery-Supercapacitor Hybrid Electrical Energy Storage Systems for Regulation Services. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 12-24.	2.5	78
59	Asymmetric Underlapped FinFETs for Near- and Super-Threshold Logic at Sub-10nm Technology Nodes. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-22.	1.8	1
60	Energy-Efficient Reduce-and-Rank Using Input-Adaptive Approximations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 462-475.	2.1	20
61	A Programmable Event-driven Architecture for Evaluating Spiking Neural Networks. , 2017, , .		16
62	Approximate memory compression for energy-efficiency. , 2017, , .		21
63	Integrated Systems in the More-Than-Moore Era: Designing Low-Cost Energy-Efficient Systems Using Heterogeneous Components. IEEE Design and Test, 2016, 33, 56-65.	1.1	20
64	EMBIRA: An Accelerator for Model-Based Iterative Reconstruction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3243-3256.	2.1	0
65	STOCK. , 2016, , .		0
66	Designing approximate circuits using clock overgating. , 2016, , .		19
67	Invited - Cross-layer approximations for neuromorphic computing: from devices to circuits and systems. , 2016, , .		30
68	Neuromorphic Computing Enabled by Spin-Transfer Torque Devices. , 2016, , .		1
69	Spin-Transfer Torque Memories: Devices, Circuits, and Systems. Proceedings of the IEEE, 2016, 104, 1449-1488.	16.4	144
70	Emulation-Based Analysis of System-on-Chip Performance Under Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3401-3414.	2.1	1
71	Asymmetric Underlapped Sub-10-nm n-FinFETs for High-Speed and Low-Leakage 6T SRAMs. IEEE Transactions on Electron Devices, 2016, 63, 1034-1040.	1.6	13
72	Cache Design with Domain Wall Memory. IEEE Transactions on Computers, 2016, 65, 1010-1024.	2.4	26

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73	Efficient embedded learning for IoT devices. , 2016, , .		19
74	High performance model based image reconstruction. , 2016, , .		18
75	Embedding Read-Only Memory in Spin-Transfer Torque MRAM-Based On-Chip Caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 992-1002.	2.1	10
76	Physiological Information Leakage: A New Frontier in Health Information Security. IEEE Transactions on Emerging Topics in Computing, 2016, 4, 321-334.	3.2	30
77	Spin-Transfer Torque Devices for Logic and Memory: Prospects and Perspectives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1-22.	1.9	153
78	Approximation through Logic Isolation for the Design of Quality Configurable Circuits. , 2016, , .		4
79	Multiplier-less Artificial Neurons Exploiting Error Resiliency for Energy-Efficient Neural Computing. , 2016, , .		16
80	Quality Configurable Reduce-and-Rank for Energy Efficient Approximate Computing. , 2015, , .		19
81	Computing Approximately, and Efficiently. , 2015, , .		25
82	Asymmetric Underlapped FinFET Based Robust SRAM Design at 7nm Node. , 2015, , .		7
83	DyReCTape: A Dynamically Reconfigurable Cache using Domain Wall Memory Tapes. , 2015, , .		8
84	SPINTASTIC: Spin-Based Stochastic Logic for Energy-Efficient Computing. , 2015, , .		23
85	Energy-Efficient Long-term Continuous Personal Health Monitoring. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 85-98.	2.5	78
86	STT-SNN: A Spin-Transfer-Torque Based Soft-Limiting Non-Linear Neuron for Low-Power Artificial Neural Networks. IEEE Nanotechnology Magazine, 2015, 14, 1013-1023.	1.1	50
87	Reliability and security of implantable and wearable medical devices. , 2015, , 167-199.		5
88	Joint Work and Voltage/Frequency Scaling for Quality-Optimized Dynamic Thermal Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1017-1030.	2.1	17
89	Approximate computing and the quest for computing efficiency. , 2015, , .		191
90	Approximate storage for energy efficient spintronic memories. , 2015, , .		60

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91	Vibration-based secure side channel for medical devices. , 2015, , .		35
92	Exploring Spin-Transfer-Torque Devices for Logic Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1441-1454.	1.9	17
93	Energy-Efficient All-Spin Cache Hierarchy Using Shift-Based Writes and Multilevel Storage. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-27.	1.8	5
94	Scalable-effort classifiers for energy-efficient machine learning. , 2015, , .		58
95	Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications. , 2015, , .		36
96	Systematic Poisoning Attacks on and Defenses for Machine Learning in Healthcare. IEEE Journal of Biomedical and Health Informatics, 2015, 19, 1893-1905.	3.9	140
97	An Application Adaptation Approach to Mitigate the Impact of Dynamic Thermal Management on Video Encoding. ACM Transactions on Design Automation of Electronic Systems, 2015, 20, 1-27.	1.9	1
98	AxNN. , 2014, , .		203
99	Trustworthiness of Medical Devices and Body Area Networks. Proceedings of the IEEE, 2014, 102, 1174-1188.	16.4	95
100	Variation Aware Cache Partitioning for Multithreaded Programs. , 2014, , .		3
101	SPINDLE. , 2014, , .		65
102	Variation tolerant design of a vector processor for recognition, mining and synthesis. , 2014, , .		3
103	StoRM. , 2014, , .		27
104	Non-Volatile Complementary Polarizer Spin-Transfer Torque On-Chip Caches: A Device/Circuit/Systems Perspective. IEEE Transactions on Magnetics, 2014, 50, 1-11.	1.2	8
105	Scalable Effort Hardware Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2004-2016.	2.1	74
106	Approximate computing for efficient information processing. , 2014, , .		0
107	Design and management of hybrid electrical energy storage systems for regulation services. , 2014, , .		13
108	Domain-Specific Many-core Computing using Spin-based Memory. IEEE Nanotechnology Magazine, 2014, 13, 881-894.	1.1	8

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109	ASLAN: Synthesis of approximate sequential circuits. , 2014, , .		22
110	STAG: Spintronic-Tape Architecture for GPGPU cache hierarchies. , 2014, , .		11
111	A defense framework against malware and vulnerability exploits. International Journal of Information Security, 2014, 13, 439-452.	2.3	10
112	STAG. Computer Architecture News, 2014, 42, 253-264.	2.5	35
113	ASLAN: Synthesis of approximate sequential circuits. , 2014, , .		18
114	Analysis and characterization of inherent application resilience for approximate computing. , 2013, , .		393
115	ROBESim: A retrofit-oriented building energy simulator based on EnergyPlus. Energy and Buildings, 2013, 66, 88-103.	3.1	33
116	Domain-wall shift based multi-level MRAM for high-speed, high-density and energy-efficient caches. , 2013, , .		1
117	Localized Heating for Building Energy Efficiency. , 2013, , .		3
118	Improving the Trustworthiness of Medical Device Software with Formal Verification Methods. IEEE Embedded Systems Letters, 2013, 5, 50-53.	1.3	33
119	Substitute-and-Simplify: A Unified Design Paradigm for Approximate and Quality Configurable Circuits. , 2013, , .		110
120	Multi-level magnetic RAM using domain wall shift for energy-efficient, high-density caches. , 2013, , .		20
121	Low-Power Digital Signal Processing Using Approximate Adders. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 124-137.	1.9	606
122	Quality programmable vector processors for approximate computing. , 2013, , .		200
123	MedMon: Securing Medical Devices Through Wireless Monitoring and Anomaly Detection. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 871-881.	2.7	174
124	Approximate computing: An integrated hardware approach. , 2013, , .		50
125	Emerging Frontiers in Embedded Security. , 2013, , .		24
126	Energy-efficient and Secure Sensor Data Transmission Using Encompression. , 2013, , .		18

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127	Energy-efficient recognition and mining processor using scalable effort design. , 2013, , .		7
128	Energy-efficient MRAM access scheme using hybrid circuits based on spin-torque sensors. , 2013, , .		0
129	Towards trustworthy medical devices and body area networks. , 2013, , .		17
130	Relax-and-retime. , 2013, , .		26
131	Managing the Quality vs. Efficiency Trade-off Using Dynamic Effort Scaling. Transactions on Embedded Computing Systems, 2013, 12, 1-23.	2.1	9
132	Reading spin-torque memory with spin-torque sensors. , 2013, , .		0
133	DWM-TAPESTRI - An Energy Efficient All-Spin Cache Using Domain Wall Shift Based Writes. , 2013, , .		63
134	Secure reconfiguration of software-defined radio. Transactions on Embedded Computing Systems, 2012, 11, 1-22.	2.1	4
135	Recovery-based design for variation-tolerant SoCs. , 2012, , .		6
136	SALSA. , 2012, , .		274
137	Guest Editors' Introduction: Green Buildings. IEEE Design and Test of Computers, 2012, 29, 5-7.	1.4	1
138	On Modeling and Evaluation of Logic Circuits under Timing Variations. , 2012, , .		17
139	Automatic generation of software pipelines for heterogeneous parallel systems. , 2012, , .		9
140	Tarazu. Computer Architecture News, 2012, 40, 61-74.	2.5	66
141	Functional analysis of circuits under timing variations. , 2012, , .		0
142	Adaptation of video encoding to address dynamic thermal management effects. , 2012, , .		4
143	Future cache design using STT MRAMs for improved energy efficiency. , 2012, , .		75
144	INVISIOS. Transactions on Embedded Computing Systems, 2012, 11, 1-20.	2.1	1

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145	TapeCache. , 2012, , .		125
146	PIC: Partitioned Iterative Convergence for Clusters. , 2012, , .		5
147	A Trusted Virtual Machine in an Untrusted Management Environment. IEEE Transactions on Services Computing, 2012, 5, 472-483.	3.2	45
148	Tarazu. , 2012, , .		133
149	Variation-Aware Voltage Level Selection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 925-936.	2.1	6
150	CLIP: Circuit Level IC Protection Through Direct Injection of Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 791-803.	2.1	18
151	VESPA: Variability emulation for System-on-Chip performance analysis. , 2011, , .		7
152	MACACO: Modeling and analysis of circuits for approximate computing. , 2011, , .		175
153	IMPACT: IMPrecise adders for low-power approximate computing. , 2011, , .		291
154	Energy efficient many-core processor for recognition and mining using spin-based memory. , 2011, , .		12
155	Dynamic effort scaling. , 2011, , .		50
156	A framework for defending embedded systems against software attacks. Transactions on Embedded Computing Systems, 2011, 10, 1-23.	2.1	1
157	MDR. , 2011, , .		19
158	Design of voltage-scalable meta-functions for approximate computing. , 2011, , .		159
159	Hijacking an insulin pump: Security attacks and defenses for a diabetes therapy system. , 2011, , .		58
160	Best-effort computing. , 2010, , .		95
161	Best-effort semantic document search on GPUs. , 2010, , .		19
162	Secure Virtual Machine Execution under an Untrusted Management OS. , 2010, , .		58

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163	A Secure User Interface for Web Applications Running Under an Untrusted Operating System. , 2010, , .		0
164	Variation-Aware System-Level Power Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1173-1184.	2.1	6
165	Scalable effort hardware design. , 2010, , .		143
166	Exploiting the forgiving nature of applications for scalable parallel execution. , 2010, , .		17
167	An evaluation of energy-saving technologies for residential purposes. , 2010, , .		14
168	Best-effort parallel execution framework for Recognition and mining applications. , 2009, , .		46
169	A framework for efficient and scalable execution of domain-specific templates on GPUs. , 2009, , .		35
170	Variation-Tolerant Dynamic Power Management at the System-Level. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1220-1232.	2.1	19
171	Coping with Variations through System-Level Design. , 2009, , .		1
172	Dynamically Configurable Bus Topologies for High-Performance On-Chip Communication. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1413-1426.	2.1	22
173	Efficient Software Architecture for IPSec Acceleration Using a Programmable Security Processor. , 2008, , .		0
174	Analysis and design of a hardware/software trusted platform module for embedded systems. Transactions on Embedded Computing Systems, 2008, 8, 1-31.	2.1	32
175	Systematic Software-Based Self-Test for Pipelined Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1441-1453.	2.1	79
176	Dynamic Binary Instrumentation-Based Framework for Malware Defense. Lecture Notes in Computer Science, 2008, , 64-87.	1.0	15
177	Energy-optimizing source code transformations for operating system-driven embedded software. Transactions on Embedded Computing Systems, 2007, 7, 1-26.	2.1	24
178	Generation of Heterogeneous Distributed Architectures for Memory-Intensive Applications Through High-Level Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1191-1204.	2.1	27
179	Hybrid Architectures for Efficient and Secure Face Authentication in Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 296-308.	2.1	7
180	Energy and Execution Time Analysis of a Software-based Trusted Platform Module. , 2007, , .		16

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181	Automated Energy/Performance Macromodeling of Embedded Software. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 542-552.	1.9	15
182	Hybrid Simulation for Energy Estimation of Embedded Software. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1843-1854.	1.9	16
183	A Synthesis Methodology for Hybrid Custom Instruction and Coprocessor Generation for Extensible Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 2035-2045.	1.9	22
184	Architectural Support for Run-Time Validation of Program Data Properties. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 546-559.	2.1	16
185	Configuration and Extension of Embedded Processors to Optimize IPSec Protocol Execution. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 605-609.	2.1	7
186	Automatic Power Modeling of Infrastructure IP for System-on-Chip Power Analysis. , 2007, , .		12
187	Aiding Side-Channel Attacks on Cryptographic Software With Satisfiability-Based Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 465-470.	2.1	15
188	Guest Editors' Introduction: Security and Trust in Embedded-Systems Design. IEEE Design and Test of Computers, 2007, 24, 518-520.	1.4	5
189	A Framework for Extensible Processor Based MPSoC Design. , 2007, , 65-95.		3
190	Accelerating System-on-Chip Power Analysis Using Hybrid Power Estimation. Proceedings - Design Automation Conference, 2007, , .	0.0	4
191	Systematic software-based self-test for pipelined processors. , 2006, , .		32
192	Hardware-Assisted Run-Time Monitoring for Secure Program Execution on Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1295-1308.	2.1	66
193	A Scalable Synthesis Methodology for Application-Specific Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1175-1188.	2.1	28
194	The LOTTERYBUS on-chip communication architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 596-608.	2.1	42
195	Software architecture exploration for high-performance security processing on a multiprocessor mobile SoC. , 2006, , .		6
196	Architectural support for safe software execution on embedded processors. , 2006, , .		19
197	Considering process variations during system-level power analysis. , 2006, , .		19
198	Design of Communication Architectures for High-Performance and Energy-Efficient Systems-on-Chips. , 2005, , 187-222.		8

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199	Enhancing security through hardware-assisted run-time validation of program data properties. , 2005, , .		1
200	Efficient fingerprint-based user authentication for embedded systems. , 2005, , .		22
201	SECA. , 2005, , .		48
202	Automated energy/performance macromodeling of embedded software. , 2004, , .		20
203	Power analysis of system-level on-chip communication architectures. , 2004, , .		51
204	Security in embedded systems. Transactions on Embedded Computing Systems, 2004, 3, 461-491.	2.1	374
205	Security as a new dimension in embedded system design. , 2004, , .		190
206	Analyzing the energy consumption of security protocols. , 2003, , .		157
207	High-level macro-modeling and estimation techniques for switching activity and power consumption. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 538-557.	2.1	28
208	Emerging Challenges in Designing Secure Mobile Appliances. , 2003, , 103-127.		0
209	System design methodologies for a wireless security processing platform. Proceedings - Design Automation Conference, 2002, , .	0.0	36
210	High-level synthesis of distributed logic-memory architectures. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2002, , .	0.0	6
211	Fast system-level power profiling for battery-efficient system design. , 2002, , .		1
212	Synthesis of custom processors based on extensible platforms. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2002, , .	0.0	60
213	Securing wireless data. , 2002, , .		64
214	Cosimulation-based power estimation for system-on-chip design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 253-266.	2.1	37
215	Battery life estimation of mobile embedded systems. , 2001, , .		153
216	Power analysis of embedded operating systems. , 2000, , .		65

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217	Behavioral synthesis of fault secure controller/datapaths based on aliasing probability analysis. IEEE Transactions on Computers, 2000, 49, 865-885.	2.4	25
218	Power management in high-level synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1999, 7, 7-15.	2.1	29
219	Design for Testability Techniques at the Behavioral and Register-Transfer Levels. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 79-91.	0.9	4
220	Verification of RTL generated from scheduled behavior in a high-level synthesis flow. , 1998, , .		19
221	Transforming control-flow intensive designs to facilitate power management. , 1998, , .		3
222	Incorporating speculative execution into scheduling of control-flow intensive behavioral descriptions. , 1998, , .		25
223	High-Level Power Analysis and Optimization. , 1998, , .		178
224	Hierarchical test generation and design for testability of ASPPs and ASIPs. , 1997, , .		8
225	Power management techniques for control-flow intensive designs. , 1997, , .		16
226	Glitch analysis and reduction in register transfer level power optimization. , 1996, , .		19
227	STeP-CiM: Strain-Enabled Ternary Precision Computation-In-Memory Based on Non-Volatile 2D Piezoelectric Transistors. Frontiers in Nanotechnology, 0, 4, .	2.4	2